HANDBOOK OF PLASMA IMMERSION ION IMPLANTATION AND DEPOSITION

Edited by

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SEMICONDUCTOR APPLICATIONS

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11.1 INTRODUCTION

Plasma immersion ion implantation (PIII) excels in large-area processing because of the high implantation dose rate and instrument simplicity. The obvious advantages are lower production time and cost. It is therefore an excellent alternative to conventional ion implantation in a number of areas pertaining to semiconductor processing [1–5]. However, since the PIII technique does not involve ion mass separation, the plasma and ionization conditions must be specifically chosen for each individual application. For instance, in order to avoid contamination, it is desirable to have the reactor wall constructed with materials compatible with semiconductor processing, for example, quartz or aluminum.

Demonstrated PIII processing for semiconductors are summarized in the dose–energy "phase space" displayed in Figure 11.1 [6–8]. Plasma doping in the low-energy regime is attractive to deep submicrometer, large-diameter Si wafer processing or thin-film transistor (TFT) technology used to fabricate flat-panel displays. These doping applications require high dose rates but noncritical as-implanted depth profiles. PIII is well suited although the

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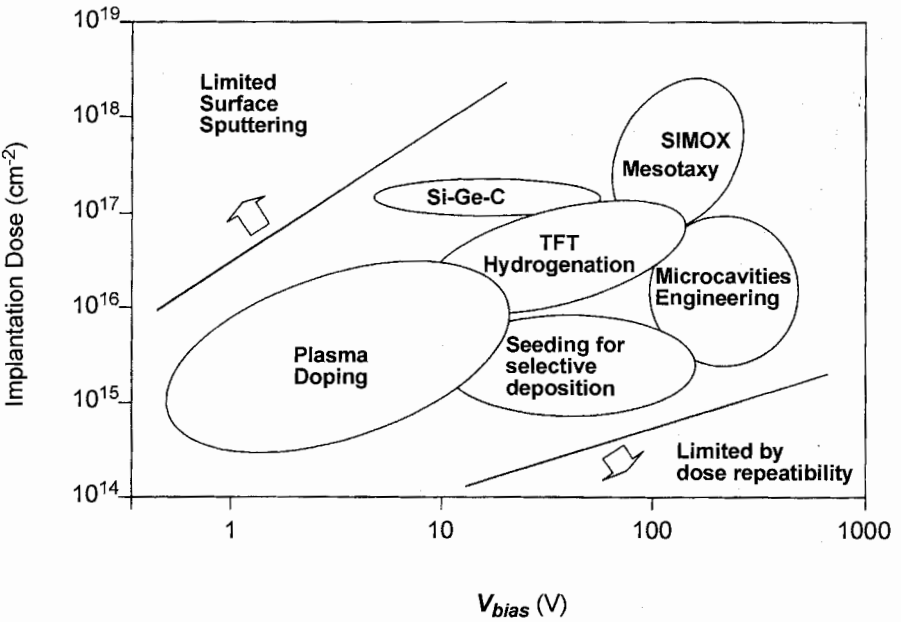

Figure 11.1 Phase space showing the dose–voltage range for various PIII semiconductor applications.

implanted species consist of nonmonoenergetic and multiply charged ion components. For instance, the final junction depth of sub-100-nm $p+/n$ junctions* depends more on the postannealing thermal cycle than the detailed shape of the as-implanted dopant depth profile [9, 10]. Since nondopant components from the plasma source (e.g., F and H) have high diffusivities during the postimplantation annealing cycle, they will escape through the surface and not pose a problem for the finished devices. Dopant implantation into polycrystalline silicon or silicides as predeposition sources and hydrogenation of polysilicon TFT also do not require critical as-implanted profiles. In the high-dose regime, material synthesis such as silicon-on-insulator [11–17], Si–Ge–C alloying [18], and microcavity engineering [19, 20] have been reported. Other applications pertinent to semiconductor processing are selective electrodeless plating of copper interconnects in SiO_2 trenches by Pd and Pd/Si seeding [21, 22] as well as backside gettering of metallic impurities in silicon [23]. It should be noted that in the low-energy regime (~ 1 kV), dose retention in the substrate is limited by surface sputtering. In the high-energy regime, the dose rate can be very large ($\sim 10^{12}/\text{cm}^2$ pulse), but sample heating, lateral uniformity, and dose repeatability are important factors.

*The notation $p+$ is commonly used to describe a heavily doped p-type layer, as opposed to p for medium doped and $p-$ for lightly doped, respectively. The notation $p+/n$ means a heavily doped p-type layer on an n-type substrate.

11.2 SHALLOW JUNCTION FORMATION

Shallow source/drain junctions (< 100 nm) for metal–oxide semiconductor (MOS) transistors can be fabricated by a number of traditional means. For $p+/n$ junction formation, high-dose ($> 10^{15}$ atoms/cm^2), low-energy (< 5 keV) BF_2^+ implantation is preceded by preamorphization of the crystalline substrate to minimize ion channeling. However, conventional beamline implanters are incapable of producing high beam currents at such low accelerating voltages. Alternatively, dopants can be introduced in the overlying polysilicon or silicide layers and driven into the substrate thermally [24–27]. Another viable technique is molecular layer doping [28–30]. Laser-based techniques such as pulsed excimer laser deposition [31], gas immersion laser doping (GILD), and projection-gas immersion laser doping (P-GILD) [32, 33] have also been shown to produce encouraging results.

11.2.1 Shallow Junctions Formed by PIII

Plasma immersion ion implantation is an attractive approach to fabricate shallow junctions because the implantation voltage can be made very low (< 1 kV) and, unlike conventional ion implantation, beam focusing is not compromised at low energy. Sub-100-nm $p+/n$ junction formation can be accomplished by preamorphization followed by PIII [34–36]. Preamorphization and doping can be carried out sequentially in the same PIII chamber without breaking vacuum using a two-step implantation process. A heavy ion (F or Si) is implanted into a crystalline Si substrate to form an amorphous layer using a SiF_4 plasma, and it is followed by boron implantation with a BF_3 plasma. For these shallow implants, no end-of-range dislocation loops or stacking faults are detected by transmission electron microscopy after rapid thermal annealing at 1060°C for 10 s. It is believed that the interstitial Si atoms generated by these shallow implants are gettered by the surface during the postimplantation annealing step. The co-implanted fluorine diffuses out of the sample during annealing and causes no deleterious effects. Sub-100-nm $p+/n$ junctions fabricated in such a way typically show a diode ideality factor of 1.05 and bulk leakage current density of about 2 nA/cm^2.

Alternatively, shallow junctions can be fabricated by a single PIII step. As exhibited in Figure 11.2, when using a BF_3 plasma at bias voltages of −2.5, −3.5, and −5.0 kV, the junction depths as determined by secondary ion mass spectrometry (SIMS) are 80, 100, and 130 nm, respectively [10]. The as-implanted junction depth of 130 nm for the 5.0-keV implant is deeper than that predicted by the Lindhard, Scharff, and Schiott (LSS) theory (Section 3.1.4) and it can be attributed to a "knock-on" process among the implanted ions. It should also be noted that the boron distributions deviate slightly from those predicted by conventional SUPREM [37] simulation due to the wider ion energy distribution during the PIII process caused by the ion–neutral charge-transfer collisions when ions move through the plasma sheath [38]. After rapid

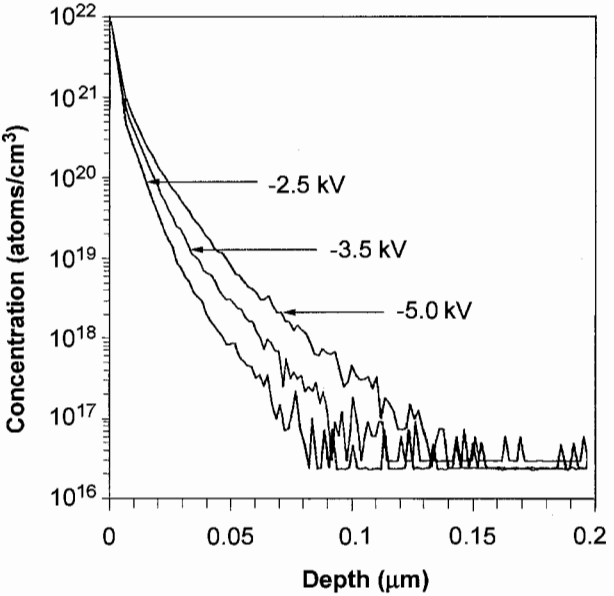

Figure 11.2 Boron in-depth distributions obtained by SIMS for samples implanted with 2×10^{15} cm^{-2} BF_2 at bias voltages of −2.5, −3.5, and −5.0 kV, respectively.

thermal annealing from 900 to 1050°C for about 10 s, the junction depths obtained are less than 100 nm (Fig. 11.3). A correlation between junction depth and implantation voltage is apparent, even though the data come from three different analytical methods. The spread of the data is due mostly to variation in annealing cycles. The lateral uniformity is also quite good. By using sheet resistance mapping, the 1-sigma uniformity of a 150-mm diameter wafer implanted with 2×10^{15} atoms/cm^2 at 3.5 kV in a BF_3 plasma is 2.4% (mean sheet resistance is 140 Ω/square).

The feasibility of integrating plasma doping into a *p*-channel metal–oxide–semiconductor (PMOS) process has been demonstrated [36]. The PMOS process has a minimum design dimension of 2 μm and gate oxide thickness of 65 nm. The PIII of BF_3 is used to dope the *p*+ source/drain and also the *p*+ polysilicon gate. The subthreshold swing of the transistors fabricated is 66 mV/decade and both PMOS inverter and PMOS NOR circuits are successfully fabricated. The electrical properties of 0.17-μm PMOSFET devices using gas source and solid source plasma doping have also been studied [5, 39]. The reverse-bias leakage current and subthreshold swing compare well with those formed by conventional low-energy ion implantation (Figs. 11.4 to 11.6). Although plasma doping inevitably introduces undesired species such as hydrogen and helium, no harmful effects have been observed. In the example shown in Figure 11.6, both the plasma and conventional junctions show similar

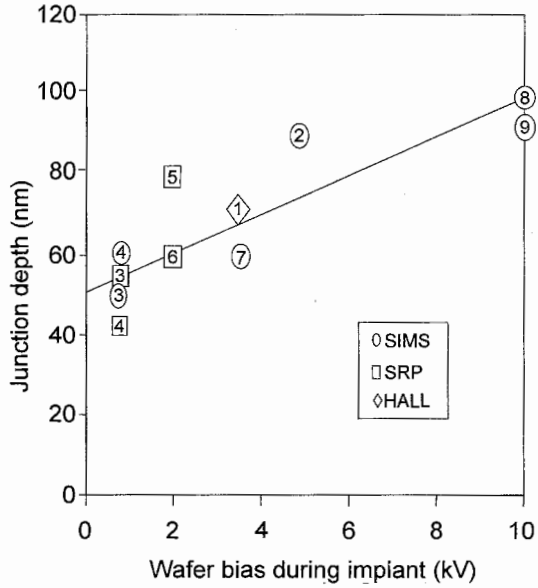

Figure 11.3 Junction depths (x_j) of PIII-doped junctions are plotted against the reported bias voltage of the implant. Data include junction depths measured by secondary ion mass spectrometry (SIMS), spreading resistance profiling (SRP), and Hall effect depth profiling (HALL). The background concentration was chosen as $10^{18}\,cm^{-3}$ to define the junction depth. Data from 1, [108]; 2, [10]; 3, [109]; 4, [110]; 5, [9]; 6, [34], 7, [111]; 8, [46]; 9, [112].

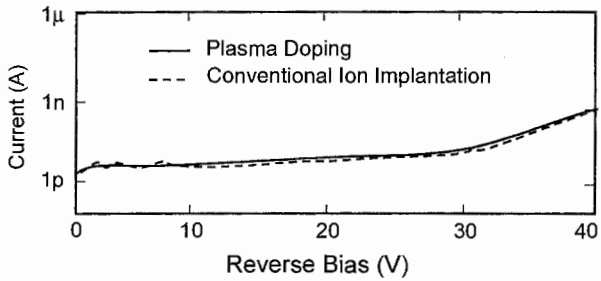

Figure 11.4 Reverse-bias diode characteristics. The plasma doped $p+/n$ diode characteristics are comparable to those of a conventionally BF_2 implanted one at 30 kV.

short-channel effects. The threshold voltage for the 0.17-μm PMOS is found to be −0.3 V.

11.2.2 Plasma Immersion Ion Implantation of BF_3/SiF_4

BF_3 gas is sometimes preferred over B_2H_6 as a boron source to fabricate $p+/n$ junctions by PIII due to its reduced toxicity. However, because of the presence

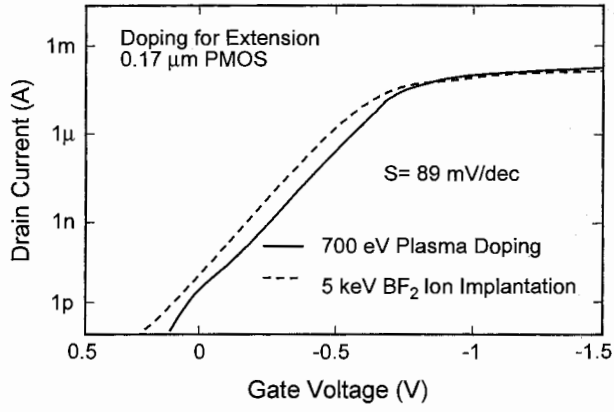

Figure 11.5 Subthreshold characteristics of 0.17 μm PMOSFET. The extensions are fabricated by plasma doping of boron at 700 eV and low-energy BF_2 ion implantation at 5 kV. The plasma doped FET shows good characteristics.

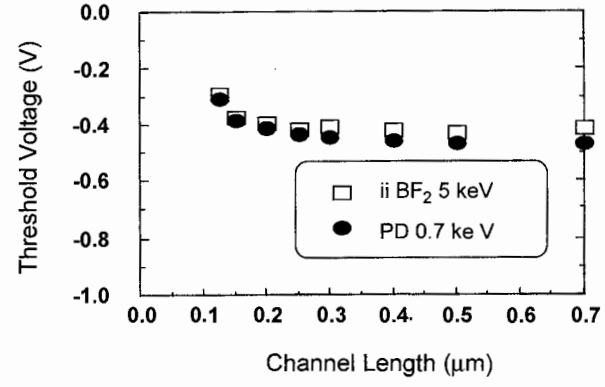

Figure 11.6 Comparison of short channel effects on the FET fabricated by plasma doping (PD) and conventional low-energy ion implantation (ii). Very little difference can be observed in the sub-250-nm region.

of reactive species in the BF_3 and SiF_4 plasmas, simultaneous etching of the target and deposition on the substrate can result during the implantation process (Fig. 11.7). Surface etching or deposition reactions must therefore be considered. A simple mathematical model [40] has been developed to predict the final depth distribution in the presence of etching and deposition:

$$Q = \frac{\Phi L}{v}\left[1 - \exp\left(\frac{-vt}{L}\right)\right] \tag{11.1}$$

where Q is the implant dose, Φ is the implant dose rate, L is the characteristic depth determined by the implant species and energy, v is the velocity of

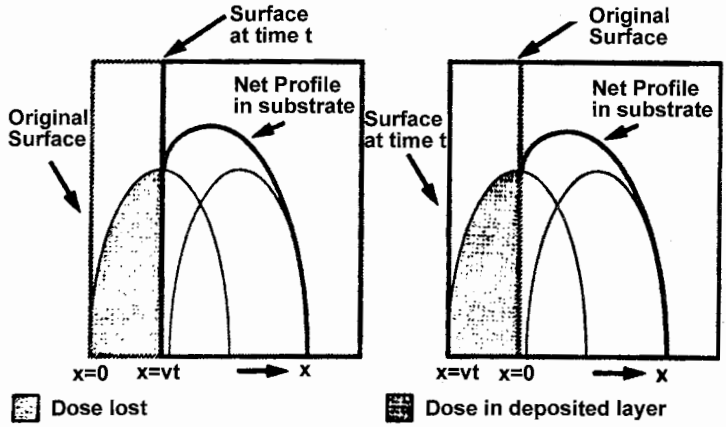

Figure 11.7 Schematic demonstration of simultaneous implantation/etching (left) and implantation/deposition (right) during PIII and the effect on the retained dose in the substrate.

interface movement, and t is the implant time. The results show that as the implantation time t becomes large in comparison with L/v, the implant dose Q will saturate, and further implantation will not increase the retained dose. For shallow junctions, the junction depth must be small, and it is imperative that v be made small by careful processing. In general, under high dose rate implantation ($> 10^{12}\,\text{cm}^{-2}\,\text{s}^{-1}$), a high retained dose can be accomplished even in the presence of etching.

For a high-dose, low-energy implant, it is desirable to work at a high plasma power to achieve maximum plasma density and a moderate pressure to reduce surface etching. There is also no strong correlation between the etching rate and the pulsing frequency, which can thus be increased to minimize etching. The total silicon etched after both SiF_4 preamorphization and BF_3 doping is less than 4 nm, as measured by transmission electron microscopy (TEM), and the SiO_2:Si selectivity factor ratio is approximately 5. The surface roughness of the etched Si surface is 4 to 5 times worse than that of the untreated sample based on results from atomic force microscopy (AFM). On the other hand, etching is quite substantial during PIII of $CoSi_2$, which is an attractive material for SADS (silicide as a doping source). Rutherford backscattering (RBS) analysis shows that up to 89% of the original Co atoms are removed from the 14-kV implanted sample.

The loss of dopants during BF_3 PIII has been determined by both SIMS and a theoretical model [41]. The boron dose versus implantation time is displayed in Figure 11.8 showing the nonlinear dose–time relationship results from the etching of the silicon by fluorine.

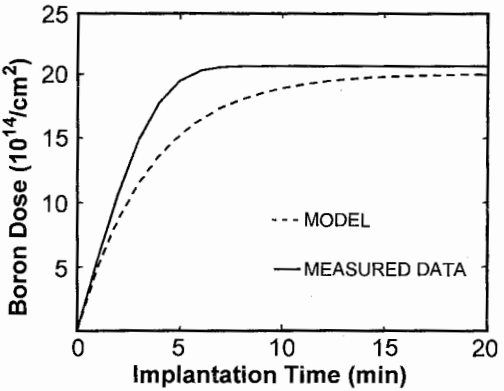

Figure 11.8 Boron dose in Si versus implantation time during BF_3 PIII.

In amorphous substances, the distribution of implanted dopant atoms about the mean projected range R_p can be approximated by a Gaussian function:

$$G(x) = \frac{N_d}{\sqrt{2\pi}\sigma_p} \exp\left(-\frac{(x - R_p)^2}{2\sigma_p^2} \right) \tag{11.2}$$

where N_d is the number of implanted ions per unit area, and σ_p is the projected straggle. In deriving Eq. (11.2), it has been assumed that the ions come to rest in a volume extending from $-\infty$ to $+\infty$. The semiconductor, however, extends only from 0 to $+\infty$. If the fraction of the ions that is backscattered is neglected, one arrives at a more exact expression [42]:

$$N(x) = \frac{2}{1 + \text{erf}\left(\dfrac{R_p}{\sqrt{2}\sigma_p} \right)} G(x) \tag{11.3}$$

where $\text{erf}(x)$ is the error function:

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x \exp(-t^2)\, dt \tag{11.4}$$

The distribution function $N(x)$ has been normalized, and the total dose is

$$M = \int_0^\infty N(x)\, dx = N_d \tag{11.5}$$

The integral M can be rewritten as:

$$M = A \int_0^\infty \exp\left[-B(x - R_p)^2 \right] dx \tag{11.6}$$

with

$$A = \frac{2N_d}{\sqrt{2\pi}\sigma_p\left[1 + \text{erf}\left(\frac{R_p}{\sqrt{2}\sigma_p}\right)\right]} \tag{11.7}$$

and

$$B = \frac{1}{2\sigma_p^2} \tag{11.8}$$

and M can be evaluated as follows after the variables are correspondingly replaced:

$$\begin{aligned} M &= \frac{A}{\sqrt{B}}\left(\int_0^{R_p\sqrt{B}} \exp(-t^2)\,dt + \int_0^{\infty} \exp(-t^2)\,dt\right) \\ &= \frac{A\sqrt{\pi}}{2\sqrt{B}}\left[\text{erf}\left(R_p\sqrt{B}\right) + 1\right] \end{aligned} \tag{11.9}$$

In order to develop the relationship defining the dose accumulated under the competing implant and etching processes, it is convenient to consider the whole process as a series of discrete implanting and etching steps. Assuming that the etching speed of silicon is v, PIII time is t, and step length is s, it will take $k = v\,t/s$ steps to finish the simulation. The total dose at time t can be written as:

$$\begin{aligned} D(t) = \left(\frac{vt}{s} + 1\right)\int_0^{\infty} N(x)\,dx - \int_0^{s} N(x)\,dx - \int_0^{2s} N(x)\,dx \\ - \int_0^{3s} N(x)\,dx - \cdots - \int_0^{ks} N(x)\,dx \end{aligned} \tag{11.10}$$

where the first term is the total dose contributed from all the steps if no etching process is involved, while the negative terms indicate the quantity lost for each step due to etching of silicon. The definite integrals can be evaluated through the sum of a series:

$$\int_0^{x} \exp(-t^2)\,dt = \sum_0^{\infty} \frac{(-1)^k}{(2k+1)k!}x^{2x+1} \tag{11.11}$$

or calculated as:

$$\begin{aligned} D(t) &= (k+1)M - s[N(s) + (N(s) + N(2s)) + \cdots + (N(s) + \cdots + N(ks))] \\ &= (k+1)N_d - s\sum_{n=1}^{k}(k - n + 1)N(ns) \end{aligned}$$

$$= (k+1)N_d - sA\sum_{n=1}^{k}(k-n+1)\exp[-B(ns-R_p)^2] \qquad (11.12)$$

Here, N_d is the dose for each step, which can be determined approximately through a short time implantation.

The measured etching speed, v, for silicon is 2.84 nm/min at $E = 10$ keV. Because BF_2^+ is the most dominant species in the plasma, the average energy of the boron dopant is 2.2 keV. At this energy, the mean projected range R_p is 0.01 μm and $\sigma_p = 0.005$ μm as calculated by the computer program TRIM [42, 43]. Simulation results with a step length $s = 0.01$ nm are depicted in Figure 11.8. The curve indicates that the total boron dose should be saturated at $2.1\times10^{15}/cm^2$ after 7 min, which is in very good agreement with the measured boron dose. As a comparison, Figure 11.8 also shows the dose–time relationship that is calculated from the simple model given in [40], where the as-implanted exponential profile is suggested. The curve exhibits the dose saturation behavior correctly, but the agreement is not as good for short implantation times. The boron profile measured by SIMS (Fig. 11.9) indicates that most of the boron is distributed within 10 nm with the peak concentration at a depth of less than 5 nm. This distribution is obviously ascribed to the etching process. As shown in Figure 11.10, the simulation curve *a* represents the boron profile if silicon was not etched away, while the simulation curve *b* gives the resultant profile when implanting and etching occur simultaneously.

Surface etching during reactive PIII has to be considered in the dose control of the process. The accumulated dose increases nonlinearly with processing

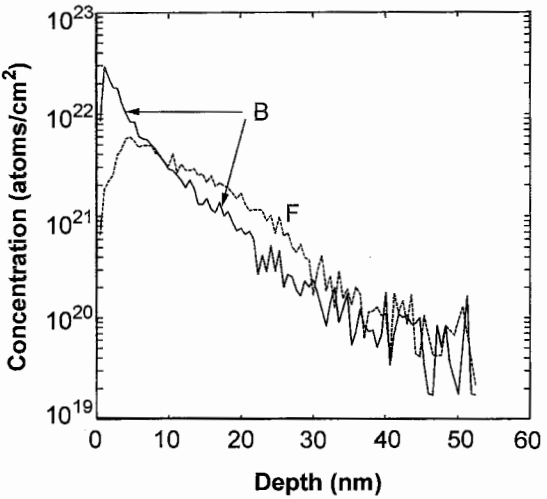

Figure 11.9 Boron and fluorine profiles in Si by SIMS.

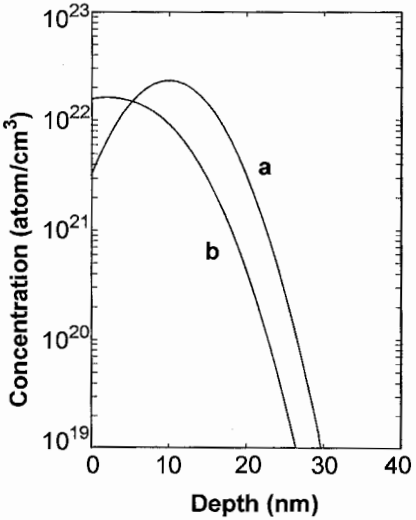

Figure 11.10 Simulated profiles of boron dopant. Curve *a* would be the profile if there were not etching during implantation. Curve *b* is the profile if implantation and etching occur at the same time.

time and eventually becomes saturated. The derived dose–time relationship can be used generally, as long as the Gaussian distribution of the as-implanted profile remains valid. The etching of the silicon surface may be mistakenly perceived to be favorable for shallow junction formation. However, since the formation of the drain region is after the polysilicon gate deposition, the effective junction depth will still be the sum of the etching depth plus the implantation depth. Such results tend to favor the use of noncorrosive gas such as B_2H_6 in shallow junction applications.

11.2.3 Doping Using Hydrides

The hydrogen etching rates of Si, polysilicon, and SiO_2 when gases such as B_2H_6, PH_3, and AsH_3 are used have been investigated [44, 45]. Without high-voltage pulsing, the etching rates are less than 0.5 nm/min for all materials and are independent of substrate temperature. However, when high-voltage pulses are applied to the substrates, the etching rates increase substantially and with temperature (Fig. 11.11). As the mass of hydrogen is small, sputtering is probably not the dominant etching mechanism and the phenomenon is attributed to reactive chemical etching by hydrogen radicals:

$$\mathrm{Si} + 4\mathrm{H} \rightarrow \mathrm{SiH_4(gas)}$$
$$\mathrm{SiO_2} + 4\mathrm{H} \rightarrow \mathrm{SiH_4(gas)} + \mathrm{O_2}$$

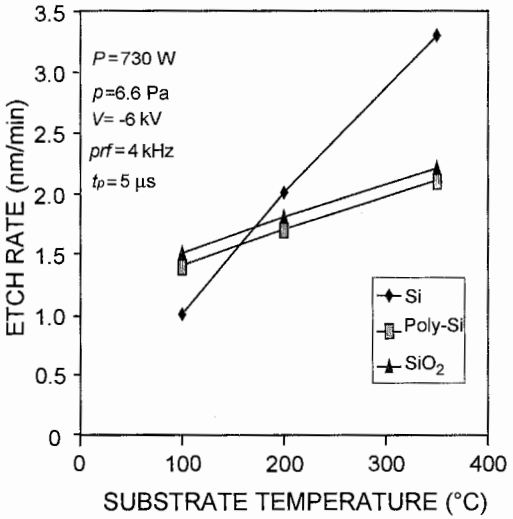

Figure 11.11 Hydrogen etching rates of Si, polysilicon, and SiO_2 versus substrate temperature with a pulse voltage of −6 kV, pulse width t_p= 5 μs, and PRF = 4 kHz.

This hydrogen etching effect can alter the structure of shallow junctions and the retained dose. The retained dose, $D(t)$, can be simulated by [40]:

$$D(t) = (k+1)N_d - \sum_{n=1}^{k}(k-n+1)N(ns) \tag{11.13}$$

where $k = vt/s$, v is the etching rate, t is the implantation time, s is the simulation step length, N_d is the dose for each step, which can be calculated by the dynamic sheath model [38, 46–49], and $N(ns)$ is the revised Gaussian implant profile after taking etching into account. Figure 11.12 displays the computed dose–time dependence. It shows that the accumulated hydrogen dose during hydrogen PIII increases nonlinearly with time and ultimately reaches a plateau when the implant dose rate is equal to the dopant loss rate due to etching.

11.2.4 Contamination Studies

The presence of impurities can be detrimental to devices, for instance, leakage currents across p/n junctions. As discussed previously, there are no filtering and collimating elements in a PIII instrument, and contaminants indigenous to the plasma or sample chamber can be easily co-implanted. In addition, effects such as etching and polymerization caused by fluorine-containing species in BF_3 PIII may affect the device characteristics [50, 51]. Figure 11.13 displays the SIMS depth profiles of H, He, and B in a silicon wafer that was immersed in a

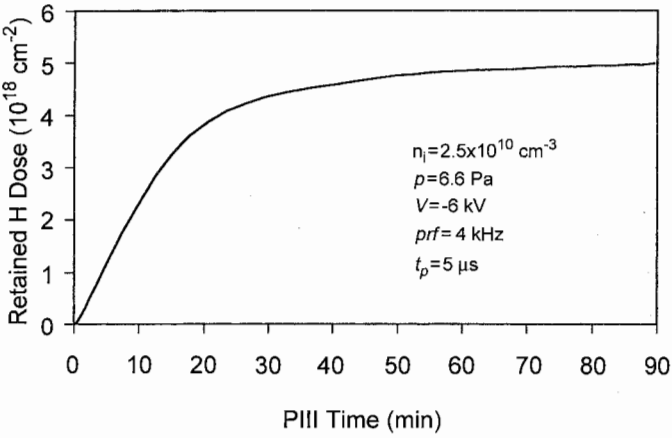

Figure 11.12 Dependence of the retained hydrogen dose on the PIII time.

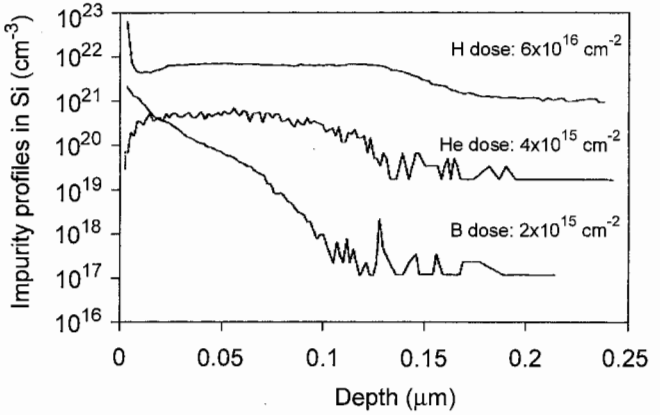

Figure 11.13 H, He, and B depth profiles in silicon by SIMS measurements (PIII parameters: bias = −10 kV, PRF = 500 Hz, t_p = 20 μs, implantation time = 10 min, pressure = 6 Pa, and microwave power = 600 W).

600-W B_2H_6/He (1%) plasma (50 mTorr) and biased to −10 kV for 10 min. Even though the H and He concentrations are significant, they do not influence the device characteristics as they are fast diffusants, and therefore very little will remain in the substrate after a high-temperature annealing step. For instance, at 1100°C, the diffusion coefficients of H and He are 10^{-6} and 1.8×10^{-4} cm^2/s, respectively, as compared to 1.5×10^{-13} cm^2/s for boron [50]. Moreover, neither helium nor hydrogen possesses energy levels in the silicon band gap and so no electrical activity, either shallow or deep, should result.

Contamination by sodium, aluminum, and iron may impact the performance of the devices more severely. It has been observed in a B_2H_6/He experiment that the sodium and iron doses are $6.0\times10^{11}\,cm^{-2}$ and $4.1\times10^{12}\,cm^{-2}$, respectively [51]. The degree of sodium contamination is reasonable considering that the experiment is conducted in a class-10000 cleanroom. The iron contamination is believed to come from the exposure of the stainless steel wafer holder to the plasma and can be reduced by using a wafer holder made of materials that are more compatible. Alternatively, a thin oxide layer can be grown on the silicon wafer before PIII to shield the Fe ions from the substrate. Very little aluminum contamination (at the SIMS detection limit) can be found, although the PIII chamber is made of aluminum. The breakdown *I-V* curve of the diode is nearly ideal and the value of 150 V is close to the theoretically expected value [52] when the substrate doping concentration is 1×10^{15} atoms/cm^3 and a one-side abrupt doping profile with a cylindrical geometry is assumed. Figure 11.14 compares the measured and theoretical forward and reverse *I-V* characteristics for the PIII diode, and a low reverse current of $15\,nA/cm^2$ ($V_R=-5\,V$) is observed. The lifetimes of minority carriers are very sensitive to impurities and crystal damage [52] and can be used to evaluate the quality of the device. The lifetime values calculated from Figure 11.14 indicate that the device fabricated by PIII has reasonable impurity contamination levels, and these values are comparable to those of devices made by conventional ion implantation. The results prove that high-quality devices can be fabricated by PIII in spite of the absence of a mass separation mechanism. The 256-kb static random-access memories (SRAM) fabricated using plasma doping techniques in the late 1990s show rather low contamination and good device characteristics [53].

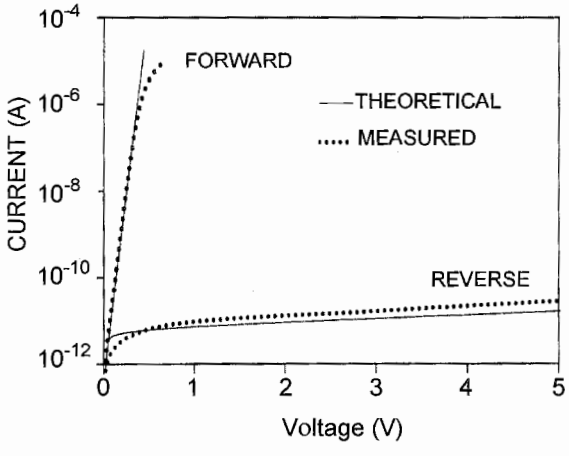

Figure 11.14 Comparison of the experimental and theoretical *I-V* characteristics of the diode fabricated by PIII.

11.3 FLAT-PANEL DISPLAYS

Plasma immersion ion implantation is used for source and drain doping or threshold adjustment during fabrication of amorphous silicon thin-film transistors (TFT). The advantages are higher throughput and self-alignment of the source/drain (S/D) regions to the gate electrode. It reduces processing steps as well as enhances the gate-to-pixel capacitance for higher image quality.

Polycrystalline silicon (polysilicon) TFT is an alternative to amorphous silicon TFT for flat-panel active-matrix liquid-crystal displays (AMLCD) because they have better device characteristics and allow for higher quality flat-panel displays (FPD) [54]. However, polysilicon TFT performance is compromised by interface traps and trap states caused by grain boundary and intragranular defects intrinsic to the polycrystalline structures. Hydrogen passivation, which has been shown to be an effective means to reduce these trap states, is commonly achieved by immersing the TFT in a plasma produced by an alternating current (AC) parallel-plate reactor [55–57] or in an electron cyclotron resonance (ECR) plasma [58–60]. Unfortunately, the relatively low ion density in an AC plasma necessitates a long hydrogenation time, whereas the sheath potential in an ECR plasma limits the hydrogen ion current to the target, thereby prolonging the processing time as well.

The PIII method is an excellent alternative passivation technique [44, 61] because of the high dose rate. Improvements in *n*- and *p*-channel device characteristics can be accomplished in 30 min using PIII while up to 8 h are required by conventional parallel-plate AC plasma immersion. Tables 11.1 and 11.2 compare the *n*-channel and *p*-channel TFT characteristics before and after 8-h conventional parallel-plate AC plasma processing, 80-min ECR plasma treatment, and 30-min, 4-kHz, −6-kV PIII. The improvement in the mobility (μ_{eff}), leakage current (I_{L}), on–off current ratio ($I_{\text{on}}/I_{\text{off}}$), threshold voltage ($V_{\text{th}}$), and subthreshold slope (S) of the 50 μm × 50 μm devices is quite obvious after hydrogen passivation, but PIII stands out on account of the much shorter processing time. In PIII, the passivation time is limited by the maximum ion

Table 11.1 Comparison of *n*-channel TFT characteristics for unhydrogenated devices, 8-h conventional parallel-plate AC plasma treatment (AC), 80-min ECR plasma treatment (ECR), and 30-min plasma immersion ion implantation (PIII)[a]

	Unhydrogenated	8-h AC	80-min ECR	30-min PIII
μ_{eff} ($\text{cm}^2/\text{V s}$)	66.9	94.5	86.3	97.6
I_L (pA)	135.4	7.8	31.2	8.3
$I_{\text{on}}/I_{\text{off}}$	1.1×10^6	5.0×10^7	1.0×10^7	4.6×10^7
V_{th} (V)	5.4	2.4	1.9	2.3
S (V/dec)	0.88	0.31	0.40	0.36

[a] μ_{eff} = effective mobility, I_L = leakage current, $I_{\text{on}}/I_{\text{off}}$ = on–off current ratio, V_{th} = threshold voltage, and S = subthreshold slope.

Table 11.2 Comparison of *p*-channel TFT characteristics for unhydrogenated, 8-h conventional parallel-plate AC plasma treatment (AC), 80-min ECR plasma treatment (ECR), and 30-min plasma immersion ion implantation (PIII)[a]

	Unhydrogenated	8-h AC	80-min ECR	30-min PIII
μ_{eff} ($cm^2/V\,s$)	48.3	56.1	68.4	56.9
I_L (pA)	−109.1	−36.8	−15.8	−13.2
I_{on}/I_{off}	9.9×10^5	2.6×10^6	2.0×10^7	1.2×10^7
V_{th} (V)	−5.0	−3.5	−1.1	−3.6
S (V/dec)	1.17	0.61	0.25	0.54

[a] μ_{eff} = effective mobility, I_L = leakage current, I_{on}/I_{off} = on-off current ratio, V_{th} = threshold voltage, and S = subthreshold slope.

density in the plasma source ($\sim 2.5 \times 10^{10}\,cm^{-3}$) and the average power of the high-voltage pulse generator. By increasing the pulse repetition rate to 15 kHz, the processing time diminishes to approximately 5 min for a dose rate of $2.0 \times 10^{15}\,cm^{-2}\,s^{-1}$. The maximum dose rate is ultimately limited by ion depletion around the substrate [62]. In practice, charge accumulation can become a factor during the time of the pulse as the devices are fabricated on an insulating quartz substrate and excessive charging can damage the devices. It is thus necessary to employ a shorter pulse width. However, citing the pulse repetition frequency as the rate-limiting factor for PIII hydrogenation assumes that diffusion from the dielectric cap into the channel and charging during the pulse will not be constraints. This is indeed the case when the pulse generator output is the limiting factor. Recent development has reduced the hydrogenation time from 30 to 5 minutes, thereby making PIII more attractive for processing polysilicon TFT materials.

The passivation mechanism for the PIII process appears to be different [61]. After hydrogen enters the device, regardless whether by conventional parallel-plate AC plasma treatment, ECR plasma processing, or PIII, it reaches the active channel by diffusion. A 10-keV H^+ ion will penetrate SiO_2 to a depth of approximately 150 nm [63], and therefore it cannot penetrate the 700-nm-thick SiO_2 cap, gate oxide, and polysilicon gate. However, the PIII hydrogen will diffuse faster as a result of the concentration dependence of diffusion. As large quantities of highly concentrated hydrogen diffuse through the device and encounter the channel defects, both the deep and the tail states will be passivated if the hydrogen concentration is large compared to the concentration of coordination defects.

11.4 SILICON-ON-INSULATOR FABRICATION

As the dimensions of modern complementary metal–oxide–semiconductor (CMOS) integrated circuits approach the sub- and deep submicrometer regimes, silicon-on-insulator (SOI) materials offer many unique advantages

over conventional silicon substrates. For instance, problems associated with alpha particles, latch-up, short-channel effects, source/drain punch-through, and hot carriers can be alleviated [64, 65]. Hence, SOI is the preferred substrate material for low-power, high-speed deep submicrometer integrated circuits, for example, 256-Mb or higher density DRAM (dynamic random-access memory) chips [66].

11.4.1 Introduction to SOI Fabrication Processes

There are currently several competing techniques to make SOI wafers. The oldest but most expensive technology is silicon-on-sapphire (SOS), which has hitherto been limited to military applications. Of the other three common SOI techniques being pursued, zone melt recrystallization (ZMR) appears to be the least desirable, whereas both SIMOX (separation by implantation of oxygen) and wafer bonding or BESOI (back-etched SOI) show promises. Unfortunately, the high cost of producing SOI wafers has prevented the technology from gaining a wider acceptance by integrated circuit (IC) manufacturers. In the case of SIMOX, the high manufacturing cost stems from the long time needed to implant a sufficient dose of oxygen into the silicon wafers, while two wafers are needed to produce one bonded SOI wafer. One industrial solution is to use ion implanters of higher current, but the associated cost is high [67, 68]. A lower-energy and lower-dose SIMOX process has been reported [69] and shows great promise for low-power electronics due to its compatibility with fully depleted field effect transistors. Again, because of its independence on wafer size, PIII is an excellent technique to produce both SIMOX and bonded SOI wafers economically [11–16].

11.4.2 SPIMOX (Separation by Plasma Implantation of Oxygen)

In the SPIMOX process, oxygen is implanted into a silicon wafer using PIII with the wafer immersed in an oxygen plasma and a negative direct current (DC) bias applied to it. At a sufficiently low chamber pressure, the mean free path of the ions is much larger than the sheath width giving an implantation energy corresponding to the applied bias voltage. Due to supersaturation of oxygen, oxide precipitates nucleate under the Si surface during the implantation. For a peaked implantation profile with an appropriate dose, these precipitates will grow and coalesce in a postimplantation high-temperature annealing process ($\sim 1300°C$) to form a continuous buried oxide (BOX) layer [70, 71]. The schematic of the SPIMOX process is shown in Figure 11.15. Figure 11.16 illustrates the significant time saving by PIII for larger wafers because the entire wafer is implanted simultaneously as opposed to the scanning technique employed for conventional beamline ion implantation. The time to implant an oxygen dose of 2×10^{17} atoms/cm^2 is about 3 min, and PIII, despite its nonbatch nature, is very attractive from a commercial standpoint.

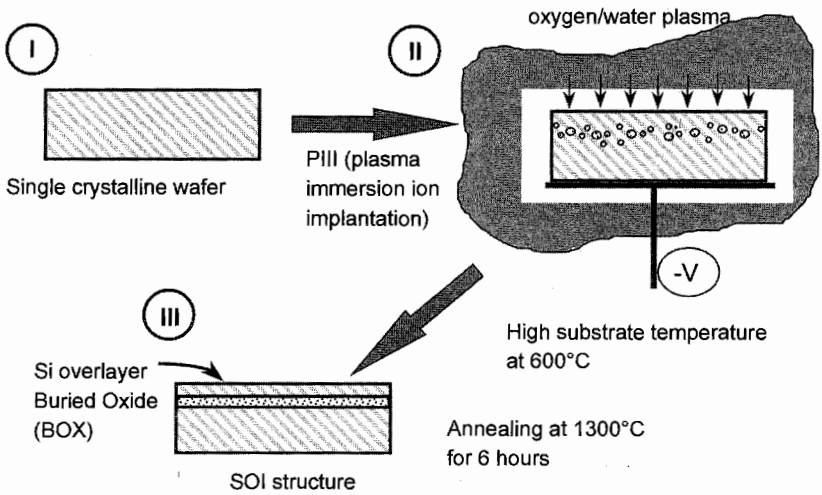

Figure 11.15 Flow chart of the SPIMOX process.

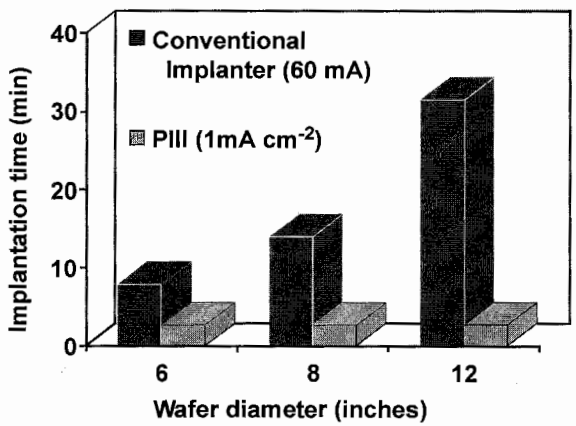

Figure 11.16 Comparison of implantation time by a 60-mA conventional beamline ion implanter and 1 mA/cm^2 PIII instrument to attain an implantation dose of 1×10^{18} atoms/cm^2.

In order to facilitate the formation of a single buried oxide layer, it is important to have a tight in-depth distribution of oxygen. Both O^+ and O_2^+ typically exist in the plasma and will be implanted. Fortunately, in the SPIMOX process, it is possible to adjust the implantation conditions such that O_2^+ is the only dominant component and a single peaked implantation profile can be achieved. For example, when employing an electron cyclotron resonance (ECR) plasma source, the plasma is composed of over 92% of O_2^+ and less that 8% of O^+. Since every O_2^+ ion carries 2 oxygen atoms, O_2^+ accounts for over 95% of the oxygen dose, while the dose due to O^+ is less than 5%. The effect of O^+ implantation is consequently unnoticeable after the

high-temperature annealing. It should also be mentioned that the substrate temperature must remain high during PIII in order to form damage-free SOI wafers. Fortunately, no sample heating is usually required because the high ion flux can heat the substrate to 550 to 600°C during implantation.

The oxygen profiles of a typical oxide-capped SPIMOX wafer before and after annealing are shown in Figure 11.17. Only one dominant peak corresponding to O_2^+ is present in the as-implanted wafer. After annealing at 1325°C for 3 h, a complete buried oxide (BOX) layer is formed. The stoichiometry of the BOX layer is identical to that of the passivation oxide layer deposited at the wafer surface. The annealed wafer also shows a sharp Si–oxide interface. A cross-sectional transmission electron microscopy (XTEM) micrograph of this annealed SPIMOX sample is exhibited in Figure 11.18. A continuous, planar buried oxide layer is present under a single-crystal Si overlayer. An atomically sharp Si–oxide interface is demonstrated in the high-resolution TEM micrograph.

Figure 11.19 illustrates the phase-space diagram in terms of oxygen pressure and implantation time [72]. Four constraints of this plasma implantation technique are shown. First, a collisionless sheath is needed to preserve single energy implantation and peaked as-implanted oxygen profile. This constraint sets an upper limit for oxygen gas pressure. Second, there is an ion density constraint imposed by the oxygen ionization efficiency and oxygen gas

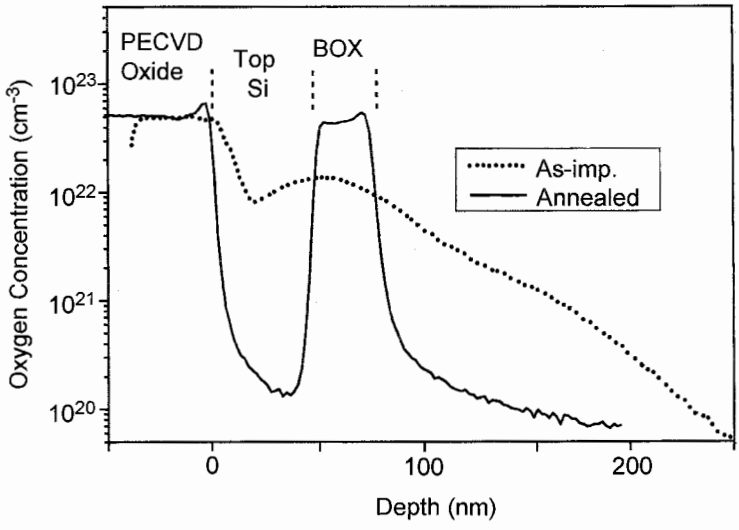

Figure 11.17 SIMS profile of oxygen in a SPIMOX wafer before and after the high-temperature annealing. Only one oxygen peak from O_2^+ implantation located near 60 nm is present in the as-implanted wafer. The O^+ peak near 130 nm is less than 5% of the total dose. After high-temperature annealing, all the implanted oxygen segregates to form the buried oxide layer with sharp silicon–oxide interfaces. The implantation is carried out at −60 kV with an oxygen dose of 1×10^{17} cm^{-2}. The wafer is then annealed at 1325°C for 3 h.

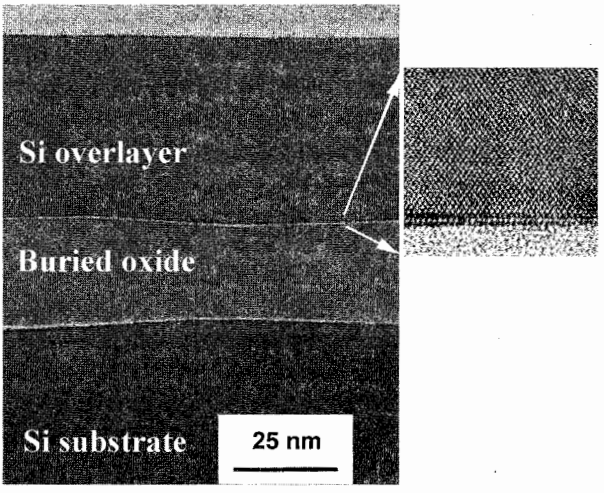

Figure 11.18 XTEM micrograph of the SOI structure formed using the SPIMOX process at 60 kV. A SOI structure with single crystalline Si overlayer thickness of 50 nm and buried oxide thickness of 25 nm is fabricated. High-resolution TEM shows (see insert) single-crystal Si overlayer is formed with atomically sharp Si–oxide interface.

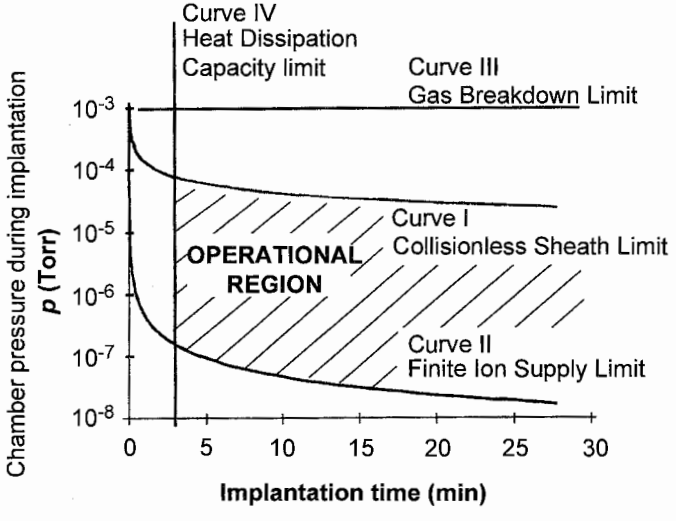

Figure 11.19 Operational phase space of the SPIMOX process. The physical limitations are: (I) collisionless sheath to preserve single energy implantation, (II) ion density limit from oxygen ionization, (III) oxygen gas breakdown at high voltage; and (IV) substrate heat dissipation capability. The curves correspond to SPIMOX conditions with a bias voltage of 100 kV and an oxygen dose of $4.4 \times 10^{17}\,\mathrm{cm}^{-2}$.

pressure. Third, there is the oxygen gas breakdown voltage constraint that sets an upper limit for the implantation voltage. The final constraint is the heat dissipation capability of the substrate that imposes a limitation to the implantation dose rate (implantation current).

Figure 11.20 shows the process window in terms of the oxygen dose and annealing temperature. If the oxygen dose is too low (less than 5×10^{16} atoms/cm^2), discontinuous oxide precipitates instead of continuous buried oxide layer are formed. A high dose (more than 3×10^{17} atoms/cm^2) causes high oxygen concentration in the overlying Si layer and leaves oxide inclusions in the overlayer. If the final annealing temperature is not high enough (less than 1275°C), the silicon–silicon oxide interfaces undulate, and the oxide thickness of SOI structures varies microscopically across the wafer.

11.4.3 SPIMOX Using a Water Plasma

As shown in the previous section, both O^+ and O_2^+ are present in an oxygen plasma. It is practically impossible to get rid of either one totally, and this can potentially cause a big spread in the implanted oxygen distribution because each oxygen atom from the O_2^+ ion only retains half of the original energy upon impact. However, the predicament can be dramatically improved if a water plasma is employed in lieu of an oxygen plasma. The most abundant ions in a water plasma are H_2O^+, OH^+, and O^+, which have masses close to each other (Fig. 11.21). Figure 11.22 exhibits the cross-section TEM micrograph of a

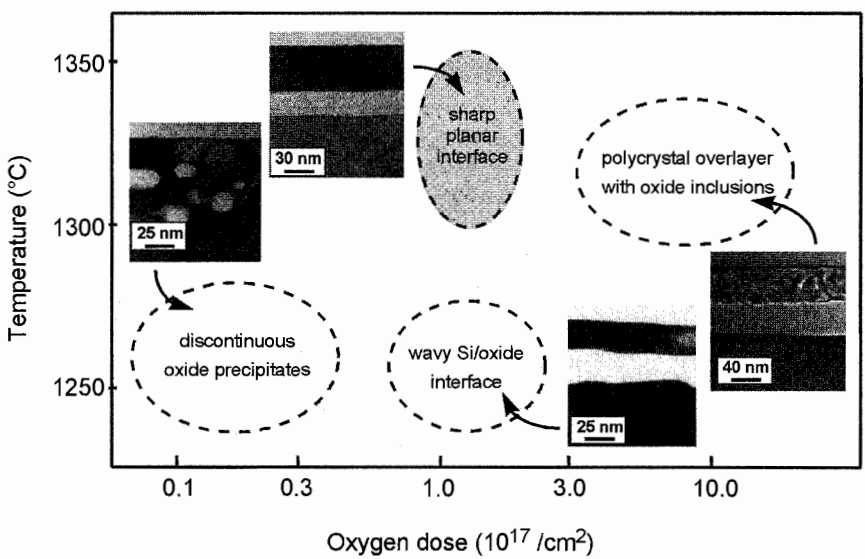

Figure 11.20 SPIMOX process window in terms of the oxygen dose and the annealing temperature. The optimal dose for −60 kV implantation is at 1 to 2×10^{17} atoms/cm^2, and the optimal annealing temperature is over 1300°C.

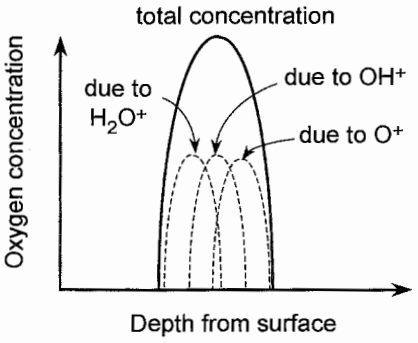

Figure 11.21 Convoluted oxygen distribution as a superposition of three implants due to H_2O^+, OH^+, and O^+. Since the three implantation ranges are quite close, the resulting peak is quite sharp, as compared to implantation with oxygen plasma.

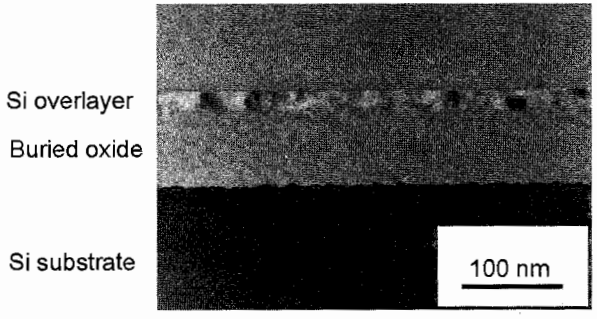

Figure 11.22 XTEM of the SPIMOX wafer formed using a water plasma: implantation dose 6.8×10^{17} cm^2, sample bias −60 kV, implantation time 20 min, annealing at 1250°C for 2 h.

sample implanted with species from a water plasma and annealed at 1250°C for 2 h. The calculated oxygen dose is 6.8×10^{17} atoms/cm^2. The silicon overlayer thickness is 30 nm and the oxide thickness is 85 nm. The silicon overlayer is polycrystalline because the wafer temperature during implantation is less than 450°C due to the low ion flux [73]. Improvement can be made if the substrate is heated during implantation and the specimen is annealed at a higher temperature and for a longer time.

11.4.4 Ion-Cut and Bonded SOI

An emerging technology, ion-cut (which is commercially referred to as Smart-Cut) is successful in producing bonded SOI wafers [74, 75]. The implantation step of the ion-cut process provides the uniformity of the top silicon thickness. The thermal growth of oxide and wafer bonding provide high-quality and excellent uniformity of the buried oxide. As shown in Figure 11.23, the process starts with two bulk silicon wafers, with one or both wafers grown with thermal

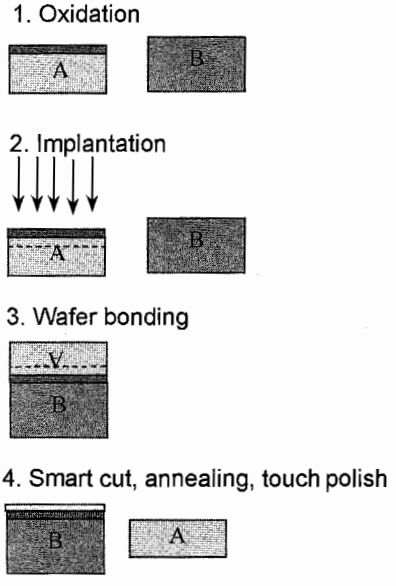

Figure 11.23 Schematic of the PIII ion-cut process.

oxide. Hydrogen is implanted into one of the silicon wafers with or without thermal oxide. The implanted wafer is then bonded with the other silicon wafer. The bonded wafer pair is then annealed between 400 and 600°C. During this thermal treatment, the wafer pair breaks into two completely separated wafers along the hydrogen-implanted region, and one of the wafers is now an SOI structure. The wafer surface is finally touch-polished to make an integrated-circuit grade SOI wafer.

The present understanding of the ion-cut process is illustrated in Figure 11.24. After hydrogen implantation, the trapped hydrogen atoms combine with silicon atoms forming a Si–H complex detectable by infrared spectroscopy measurement [76, 77]. During thermal annealing, the trapped hydrogen atoms diffuse and segregate near the peak region to form microcavities filled with H_2 molecules. Under further annealing, more hydrogen diffuses into the microcavities, and the high pressure becomes the driving force for its expansion and growth. In the first case, if a surface stiffener such as a bonded wafer is capped on the implanted wafer surface, these microcavities grow along the (100) plane parallel to the wafer surface during annealing. When they grow larger and larger, more hydrogen atoms diffuse in, keeping the internal pressure high enough for further expansion. Meanwhile, microcavities will coalesce forming even larger cavities. When all the cavities are linked together, the bonded wafer pair becomes completely separated along the cavity plane. In the second case, if no capping layer is present on the implanted wafer surface, a similar mechanism causes the microcavity nucleation and growth under

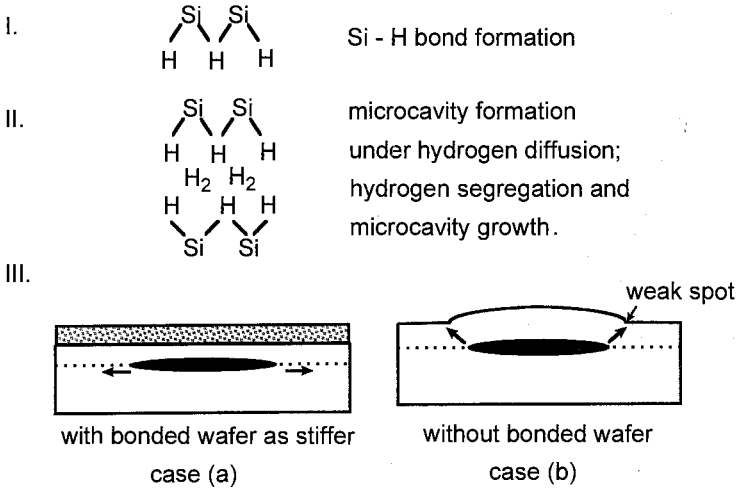

Figure 11.24 Schematic picture of current understanding of the silicon cleavage and ion-cut process.

thermal annealing. However, the microcavity expansion and growth can easily derail causing penetration through the surface layer and small, localized layer cleavage results.

For the hydrogen PIII ion-cut process, simultaneous implantation of H^+, H_2^+, and H_3^+ may initiate cleavage at different depths. By adjusting the hydrogen gas pressure, plasma power, and magnetic field, a hydrogen plasma with H^+, H_2^+, or H_3^+ as the dominating implanted species can be achieved. By simultaneously keeping the wafer temperature below 250°C, the implanted hydrogen is less likely to diffuse and nucleate during the implantation step. The secondary ion mass spectrometry (SIMS) profile of a sample implanted at 50 kV is displayed in Figure 11.25. It shows that over 95% of the hydrogen dose is from H_2^+ while less than 5% originated from H^+. The amount of H_3^+ was very low. The two hydrogen peaks in the SIMS profile are in very good agreement with TRIM92 simulations (Section 3.1.10.1), which predict a projected range of 0.296 μm for 50 keV H_2^+ and 0.493 μm for 50 keV H^+.

A $Si/SiO_2/Si$ structure formed using the hydrogen PIII ion-cut process is shown in Figure 11.26. The top silicon wafer is implanted using an H_2^+-dominated plasma at 35 kV and a nominal dose of 1×10^{17} atoms/cm^2. The wafer separation is uniform across the sample surface, and there is no silicon layer separation along the H^+ or H_3^+-implanted region. The dashed line indicates the original bonded oxide–oxide interface. It is apparent that after the 900°C, 60-min final annealing process, there is no distinguishable interface in the bonded oxide layer.

The SOI structures can also be synthesized using helium PIII ion-cut. The only dominant ion constituent is He^+, and there is no multiple ion species problem as confirmed by SIMS. A cross-section transmission electron

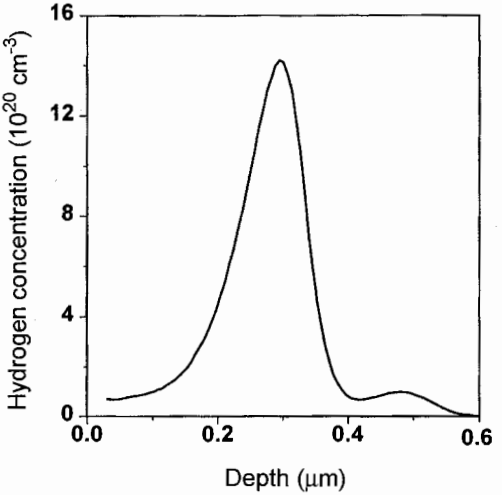

Figure 11.25 SIMS profile of implanted hydrogen using PIII. The implantation energy is 50 kV. Over 95% of the hydrogen dose is from H_2^+ ions.

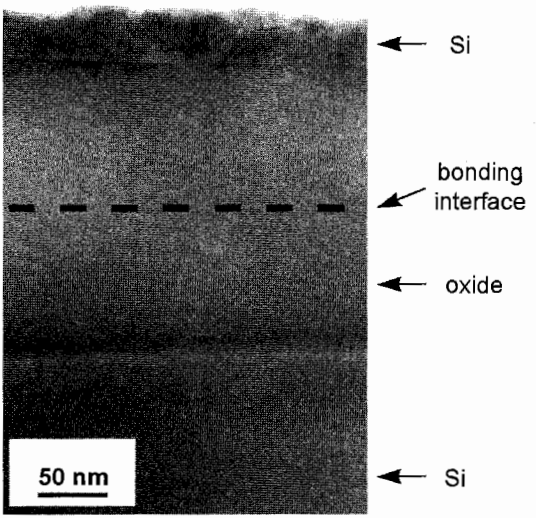

Figure 11.26 XTEM micrograph of $Si/SiO_2/Si$ structure formed using hydrogen PIII ion-cut. The top silicon wafer is implanted using hydrogen plasma at 35 kV with 10^{17} cm^{-2} nominal dose. The dashed line indicates the bonded oxide–oxide interface.

microscopy (XTEM) image showing helium-induced cleavage is exhibited in Figure 11.27. Microcavities formed along the (100) plane, very similar to that observed in hydrogen-implanted samples. Figure 11.28 shows the XTEM image of a $Si/SiO_2/Si_3N_4/SiO_2/Si$ structure. In this case, a silicon wafer with a

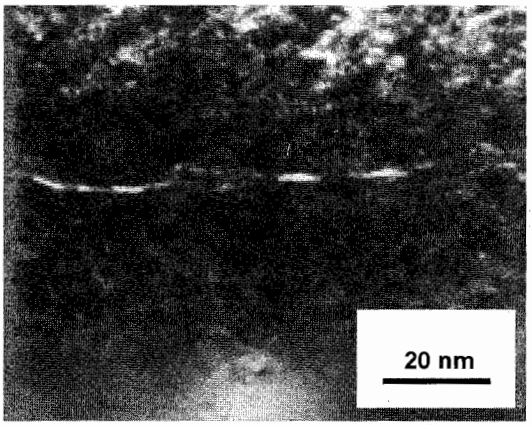

Figure 11.27 XTEM image of helium-induced microcavities inside silicon. Helium is implanted at 40 kV with a nominal dose of $10^{17}\,cm^{-2}$ using PIII. The sample is annealed at 600°C in a nitrogen ambient for 30 min.

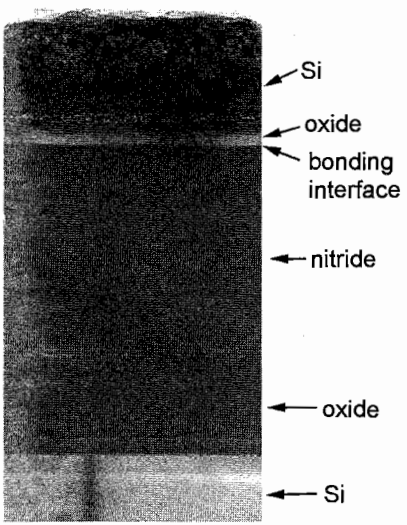

Figure 11.28 XTEM micrograph of a $Si/SiO_2/Si_3N_4/SiO_2/Si$ structure formed using helium PIII ion-cut process. The top silicon wafer is implanted using helium plasma at 33 kV with $10^{17}\,cm^{-2}$ nominal dose. The dashed line indicates the bonded oxide–nitride interface. There is extended crystal damage and microcavity formation in the silicon layers.

20-nm oxide layer was implanted with He^+ at 33 keV with a nominal dose of 1×10^{17} atoms/cm^2. It was subsequently bonded to another silicon wafer having plasma-enhanced chemical vapor deposition (PECVD)-deposited oxide and nitride layers on the surface. The implanted wafer cracked along the implanted helium peak region during subsequent 500°C annealing. This SOI structure

was finally annealed at 1100°C for 60 min to solidify the SiO_2/Si_3N_4 interface, which is indicated by the dashed line in the image. This $Si/SiO_2/Si_3N_4/SiO_2/Si$ structure demonstrates that other than oxide and silicon, other materials such as Si_3N_4 can be incorporated in the SOI structure using the PIII ion-cut process.

11.5 MICROCAVITY ENGINEERING

11.5.1 Gettering Effects

Not only has the chemistry of helium-induced or hydrogen-induced cavities spurred research activities in the ion-cut technology, but also there are other interesting phenomena such as impurity gettering and light emission [78–81] as the clean inner surface of these cavities facilitates the study of surface phenomena. The gettering characteristics of the helium PIII-induced cavities with and without oxygen precipitates have been investigated [19]. Figure 11.29 shows a cross-sectional TEM picture of these cavities of 8 to 50 nm in diameter. The SIMS depth profiles of Cu and Au are exhibited in Figure 11.30. The peak of the Cu profile is at a depth of approximately 200 nm with a width of about 240 nm corresponding to the expected cavity band (20 keV He^+ PIII). The gold profile shows a depth of 95 nm and a spread of about 110 nm, which again matches the location of the cavity band (8-keV He^+ PIII). These results

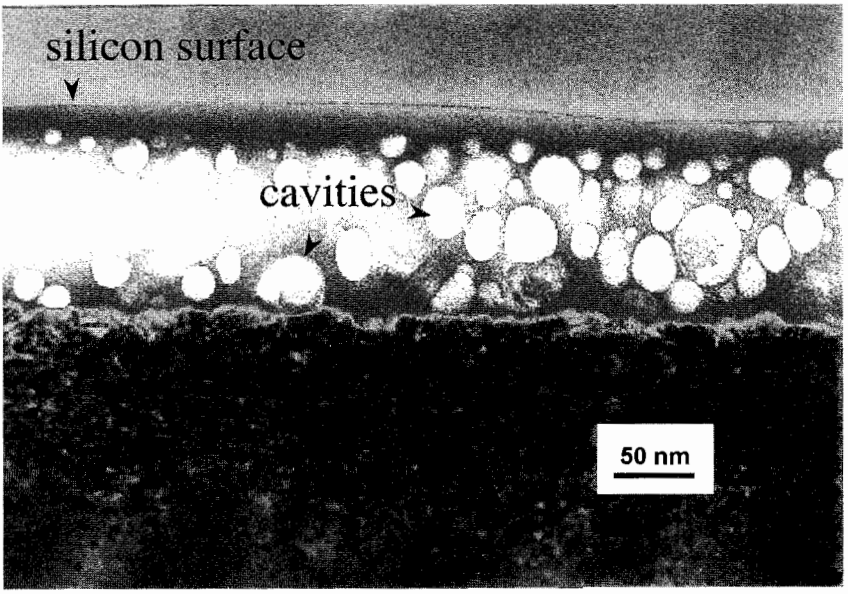

Figure 11.29 XTEM micrograph showing buried microcavities 8 to 50 nm in diameter.

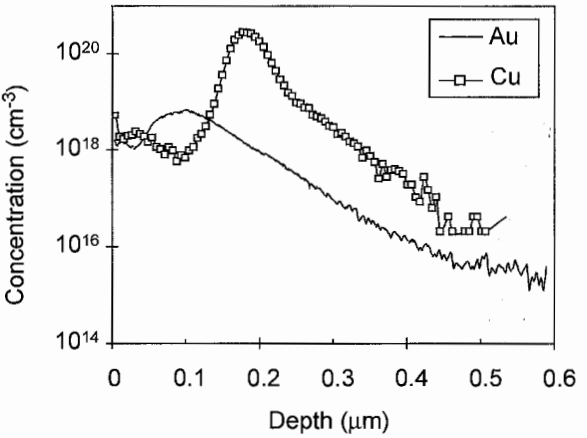

Figure 11.30 SIMS depth profiles of Cu and Au demonstrating gettering by the helium cavities. The Au-gettered sample corresponds to He^+ implantation at 8 kV. The Cu-gettered sample corresponds to He^+ implantation at 20 kV. The implantation dose in both cases is $2 \times 10^{17}\,cm^{-2}$ and the samples are annealed at 1200°C for 2 h in nitrogen.

illustrate that the well-defined band of helium-induced cavities acts as an effective gettering sink for both Cu and Au. The RBS data shown in Figure 11.31 confirm that the areal density of Cu in the copper-gettered sample is 1.9×10^{16} atoms/cm^2. In order to examine the stability of these cavities and the

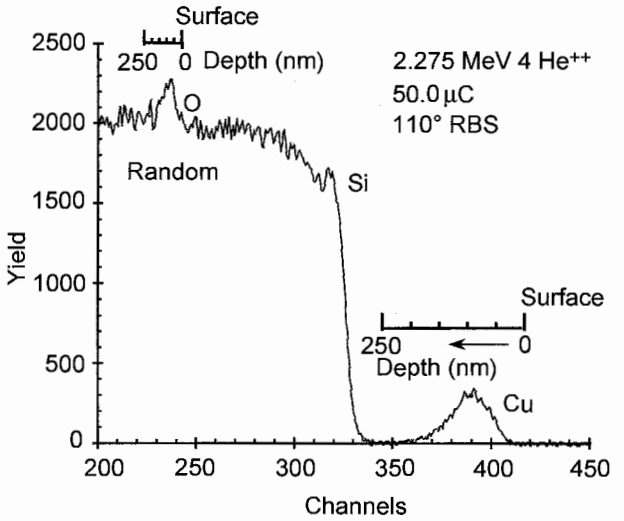

Figure 11.31 RBS spectrum for the sample implanted with $2 \times 10^{17}\,cm^{-2}$ of He^+ at 8 kV and subsequently implanted with $1.7 \times 10^{17}\,cm^{-2}$ of O_2^+ at 65 kV. Cu is diffused and gettered by two annealing cycles up to 1200°C for 2 h.

gettering process, this sample was annealed further for 2 h at 1200°C. The results show that Cu was still trapped in the helium-induced cavities even after the second high-temperature annealing step. The combination of PIII and microcavity formation is thus well suited for impurity gettering in large wafers because of the high dose rate and short implantation time.

11.5.2 Buried Light-Emitting Porous Silicon

Strong light emission from electrochemically etched porous silicon (PS) at room temperature opens the possibility of integrating optoelectronic and microelectronic devices in a single Si wafer [82]. Unlike conventional chemical etching methods, which cause a rough surface and leave surface impurities after the etching process [83], hydrogen PIII can produce buried microcavities thereby avoiding contamination from the acid, and it has better compatibility with silicon-based IC fabrication [81]. Nanosized bubbles or microcavities are formed under the surface by implanting hydrogen into a crystalline silicon wafer [19]. When the silicon walls between these bubbles are thin enough to allow quantum effects to take place, silicon will be transformed from an indirect to a direct bandgap material. It emits light at an energy greater than the energy of the indirect silicon bandgap. The material created is called buried porous silicon (BPS) since its structure is similar to ordinary porous silicon.

The photoluminescence (PL) spectrum in Figure 11.32 was acquired at an excitation wavelength of 514.5 nm. There are two broad fluorescent bands in the as-implanted sample: 1010 and 890 nm (curve *c* in Fig. 11.32). By comparing the PL spectrum with one of pure silicon acquired under the same

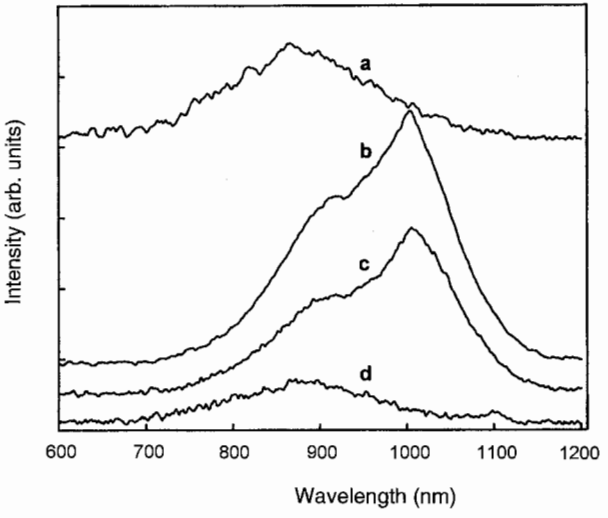

Figure 11.32 PL spectra of pure Si (curve *d*) and hydrogen implanted samples: (*a*) 670°C, 2 h annealing, (*b*) 325°C, 1 h annealing, and (*c*) as implanted.

conditions, one sees that the 890-nm peak is due to instrumental background. The small peak at 1100 nm in the pure Si PL spectrum corresponds to band emission of Si. Its energy is equivalent to the indirect bandgap of silicon. Thus, the band located at 1010 nm originates from the BPS. The full-width half-maximum (FWHM) of this band is about 0.2 eV. The BPS emission band can still be observed after annealing at 325°C for 1 h, but it almost disappears after annealing at 670°C for 2 h. This is due to the coarsening of the bubbles during the annealing process as well as the loss of hydrogen from the silicon wafer when the annealing temperature exceeds 400°C [84]. The implanted hydrogen can passivate nonradiative recombination centers stemming from defects and dangling bonds and consequently increase the efficiency of light emission.

The microcavities can be observed using XTEM (Fig. 11.33). In this sample, the projected range of BPS is about 50 nm. The Si absorption coefficient of photons at an energy of 1.5 eV is 780 cm^{-1} [85]. Therefore, the emitted light from the underlying BPS layer penetrates the thin overlay practically unattenuated. Even if the light energy shifts to 2.5 eV (blue), the transmission loss is still minimal and 91% of the fluorescent light can be transmitted. This has important ramification if indeed both photonic and microelectronic devices can be fabricated on or in the same substrate. The important advantage of this process is that BPS materials are more stable than their electrochemically etched counterparts because they are protected by the overlayer.

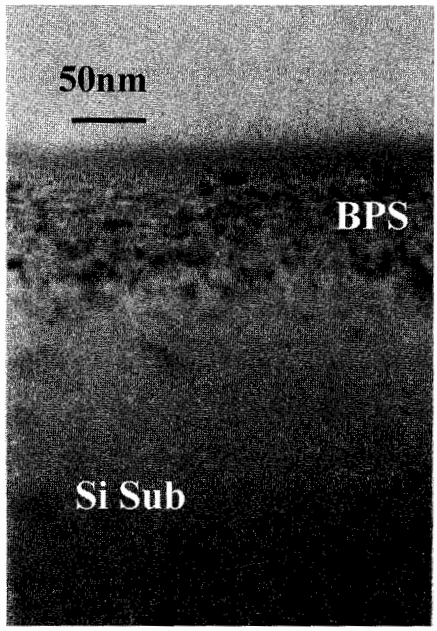

Figure 11.33 XTEM picture of buried porous silicon.

11.6 TRENCH DOPING

Three-dimensional structures such as trench DRAM provides a higher surface area for charge storage, but doping of high aspect ratio trenches poses a formidable challenge for conventional ion implantation [86, 87]. Conformal doping of trenches can be accomplished by applying a bias to the substrate placed in a radio frequency (RF) plasma of a dopant gas [88, 89]. Scattering among the ions and neutrals in the plasma provides a spread in the angular distribution of the implanted ions, and ions can be implanted into the sidewalls of the trench.

Figure 11.34 shows the stained cross sections of trenches with an aspect ratio of approximately 12 (trench opening ~1 μm) doped by boron PIII (0.6 Pa

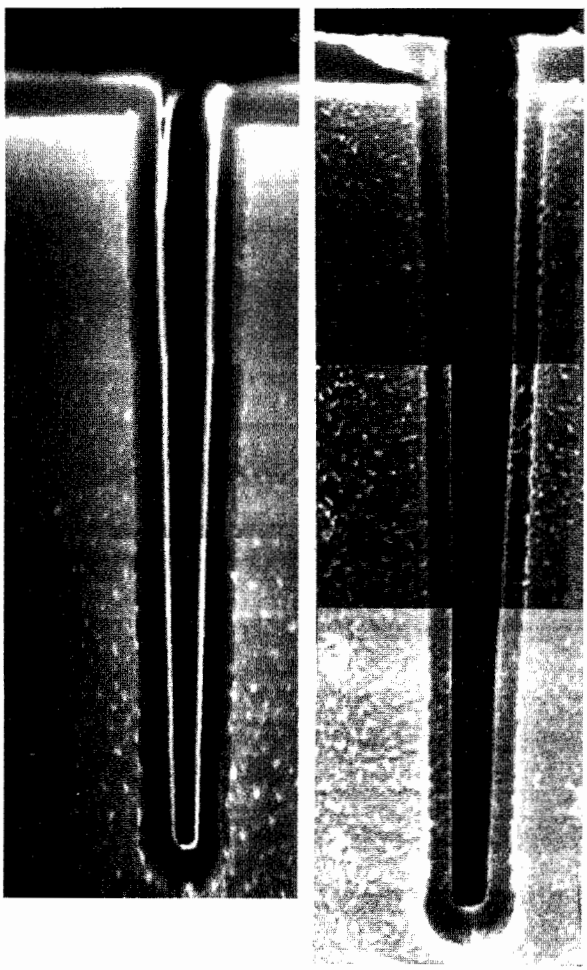

Figure 11.34 Cross-sectional SEM images of stained trench samples implanted using 0.6 Pa BF_3 at 7.5 kV (left) and 10 kV (right).

BF_3 and 5 to 7.5 kV pulse bias) [90]. No evidence of ion beam shadowing can be observed, and the junction is quite uniform along the sidewall. For doping nearly vertical trenches, dopants must receive their momentum from collisions as they traverse the ion sheath. The amount and distribution of dopants along the sidewall thus depends on the ion angular distribution. PIII is performed here in an unusual mode: The sheath width is much larger than the trench width, the characteristic feature size of the substrate. The PIII sheath develops outside the trench and ions are accelerated approximately parallel to the trench depth. For the same plasma gas pressure, greater bias will result in a lower average incident angle as ions are accelerated to higher velocities and their trajectories are more collimated. This dependence is demonstrated in Figure 11.35 in which trenches with aspect ratios 5 and 1 show a lower sidewall dose when the PIII voltage is higher. Figure 11.36 shows quantitatively the difference in the average sidewall dose (ϕ_{SW}) to surface dose (ϕ_S) ratios under

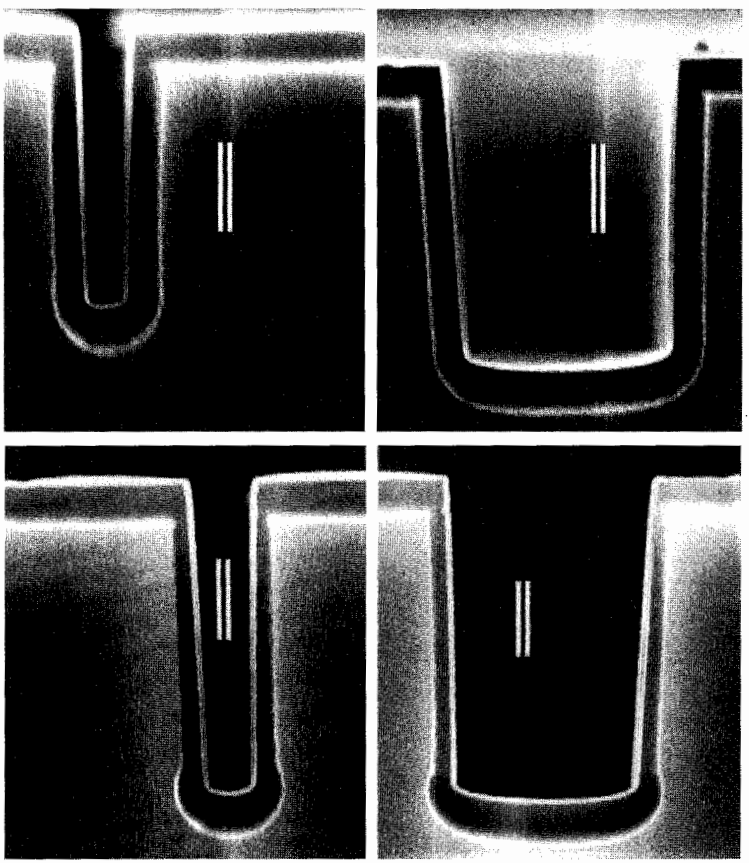

Figure 11.35 Cross-sectional SEM images of stained trench samples implanted at two bias conditions and two aspect ratios: Bias 5 kV (top), 10 kV (bottom). Aspect ratios: 5 (left), 1 (right).

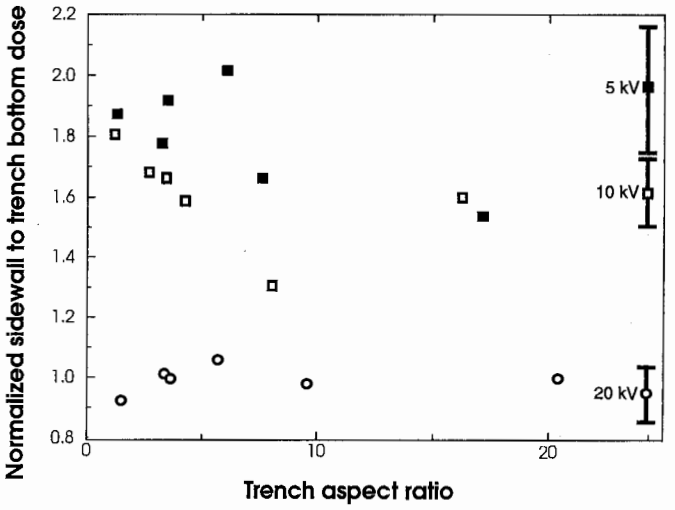

Figure 11.36 Average sidewall dose over surface dose, $\langle \phi_{SW} \rangle / \langle \phi_S \rangle$ for three bias amplitudes. Doses have been normalized to the average value for the 20-kV case. Error (±14%) bars are indicated for each sample.

three PIII bias voltages, 5, 10, and 20 kV. It is clear that the ratio is higher at a lower bias. Hence, the dose distribution along the trench sidewall can be controlled by using the appropriate combination of biases.

11.7 METALLIZATION TECHNOLOGY FOR DEEP TRENCH FILLING

The semiconductor industry's remarkable progress in miniaturization, and performance is summarized in Moore's law, which these days is interpreted as a broad statement that the time for doubling chip performance is 18 months. This progress has been enabled by an equally remarkable tradition of innovation through the years that has led to processes capable of increasing degree of miniaturization. A significant hurdle for future generations of integrated circuits (ICs) will be the "wiring" or interconnection of their internal elements. In the present 250-nm generation of ICs, aluminum is the metal of choice for in-plane interconnection, and tungsten is used for connections between layers ("vias").

The recent introduction of ICs using copper-based metallization has marked the beginning of a change from aluminum to copper metallization technology. Copper has several advantages over aluminum: its lower resistivity (1.67 Ω cm for copper versus 2.65 Ω cm for aluminum alloys) allows finer "wires" with lower resistive losses, resulting in shorter on-chip resistance–capacitance (RC)

time delays. Also, the higher mass and melting point of copper make it significantly less susceptible to electromigration (transport of atoms of the metal conductor when carrying high current densities) than aluminum, and less likely to fail under stress. Copper poisons silicon [91] and requires a diffusion barrier to prevent contamination of the active areas of the device. Tantalum and tantalum nitride thin layers prevent the diffusion of Cu in Si or SiO_2, and simultaneously improve the adhesion between Si or SiO_2 and Cu.

The present trend in IC fabrication is toward using the damascene (or dual-damascene) process. Vias and trenches are etched into dielectric layers and filled with the metal, and the component is finally chemical-mechanical polished to produce a planarized structure. Conventional physical vapor deposition (PVD) techniques such as sputter deposition and evaporation have failed to fill trenches with a high aspect ratio (depth:width). Clogging of trenches occurs before filling is complete, leaving voids inside the metallic conductors. Improved trench filling has been achieved with collimated sputtering [92] or sources that have a high degree of ionization such as self-sputtering [93], electron cyclotron resonance (ECR) [94], or vacuum arc plasma sources [95]. These methods, however, have failed to fill trenches with aspect ratios greater than 4:1 in trenches less than 180 nm wide because of inadequate control over the particle (ions and atoms) velocity distribution and ion energy.

The combination of filtered cathodic arc (FCA) and PIII, a process known as MePIIID and described in detail in Section 4.8, has proved successful in filling trenches as narrow as 100 nm and aspect ratios as high as 9:1 [96]. The ability to tailor the step coverage and the deposition mode results from the high directionality of the ion flux and the tight control of the energy of the depositing ions.

Cathodic arcs, discussed in Section 7.8, are prolific generators of highly ionized metal plasma [97, 98]. The plasma is formed at the cathode surface and is guided through a magnetic filter to eliminate "macroparticles" [99–101]. The ions are produced in the cathode plasma with energy in the range 20 to 200 eV, depending on the ion species [97]. The energy of the depositing ions is controlled by applying a repetitively pulsed negative bias voltage to the substrate.

The net deposition rate during film growth using energetic ions results from the competition between two processes—ion deposition and sputtering (Section 4.8.3). The natural condensation rate of metal ions from the plasma stream on the wafer surface depends on the particle flux magnitude and direction with respect to the substrate. The fraction of arriving particles that is retained on the surface is modified by self-sputtering, and the self-sputtering rate depends on the energy of the incident particle and on the angle of incidence. Momentum transfer to atoms at the film surface increases atomic mobility, favoring migration toward deeper locations in the trenches. The angle of incidence is very important for the filling of narrow trenches and vias because of the difference in sputtering rates of the vertical and horizontal walls of a trench or vias. In general, the sputtering yield for an incident angle β, $Y(\beta)$,

is related to the normal incidence sputtering yield $Y(0)$ by:

$$Y(\beta) = \frac{Y(0)}{(\cos \beta)^{f_s}} \tag{11.14}$$

where f_s is a function of the masses of the incident ions and of the substrate atoms; see Section 3.1.6 and [102].

The principles and techniques of the process used here are outlined in Sections 4.8 and 7.8. A detailed description of the experimental setup can be found in [103–105]. In brief, a vacuum arc plasma gun was used in a repetitively pulsed mode to generate the metal plasma. Copper and tantalum plasmas were produced using copper and tantalum cathodes, respectively. The deposition was carried out near room temperature, with the Si wafer mounted on a water-cooled substrate.

The ion energy during the process is the sum of the streaming energy with which the ions are formed and the energy added by the applied bias (Section 4.8). The streaming energy E_0 is approximately 90 eV for Cu and 180 eV for Ta [97], and thus the total energy during deposition alternates between

$$E = E_0 + \bar{Z}eV_{\text{bias}} \tag{11.15}$$

during the bias pulse-on time and

$$E = E_0 \tag{11.16}$$

during the pulse-off time, where $\bar{Z}$ is the mean ion charge state (2.0 for Cu and 2.9 for Ta [106], cf. Table 4.6), V_{bias} is the applied bias voltage, and e is the electron charge.

In conventional ion-assisted deposition, the ion:neutral ratio is an important parameter in defining the film properties and the growth pattern (Section 3.2). The equivalent parameter in the process here is the duty cycle of the bias voltage, which defines the ratio between the flux of ions with high energy, given by Eq. (11.15), and the flux of ions with low energy, given by Eq. (11.16).

Equation (4.2.3), the equation of dynamic sheath thickness derived in Section 4.2, predicts that, for the typical plasma densities at the substrate location, the dynamic sheath thickness is of the order of several tens of micrometers after 1 μs. Since the trench widths under consideration are less than 250 nm, the sheath will not exist inside the trench for any significant fraction of time. Therefore the sheath is parallel to the wafer plane, and the ion acceleration is normal to the wafer surface, yet enhancing the ion velocity component normal to the wafer surface.

Oblique incidence of the ions favor the formation of overhangs at the trench entrance, which results in uneven film thickness on the trench walls, and eventually the clogging of the trenches. This type of defect is shown in Figure 11.37. Wider trenches are obviously less susceptible to clogging. Early attempts

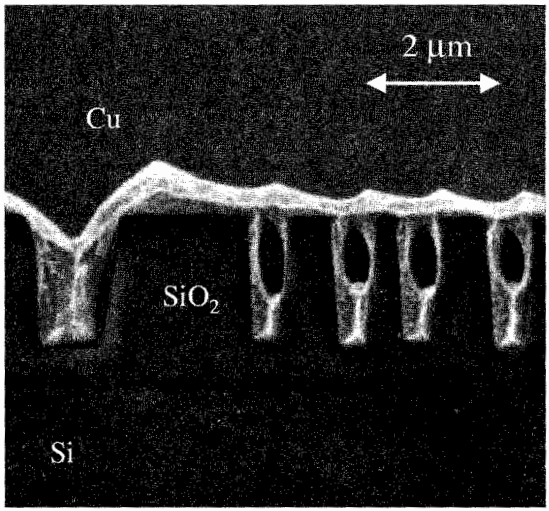

Figure 11.37 Defects produced while filling trenches. Oblique incidence of ions favors the formation of overhangs at the trench entrance resulting in clogging.

using filtered cathodic arc have failed to produce defect-free trenches with aspect ratios greater than 4:1 [95, 107] for not recognizing the importance of optimizing the condensation-to-sputtering ratio. When the deposition is carried out using a bias voltage of −100 V and a duty cycle of 50%, it is possible to achieve deposition of Cu trenches with much higher aspect ratios, and the

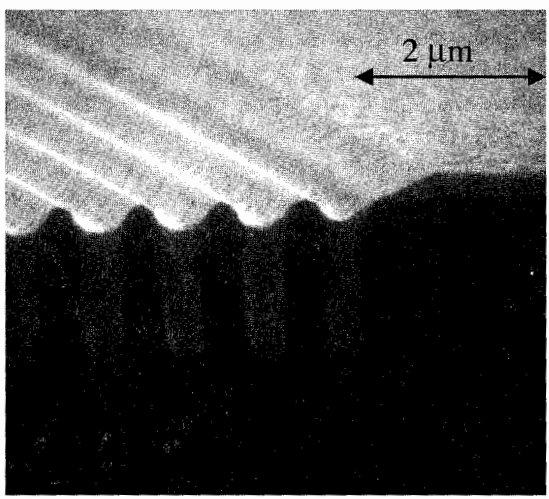

Figure 11.38 Trenches filled with void-free copper using cathodic arc copper plasma and bias voltage of −100 V at a duty cycle of 50%.

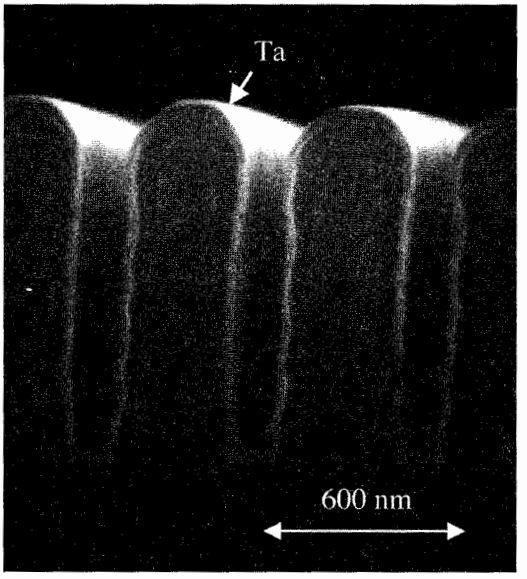

Figure 11.39 Deposition of a highly conformal 20-nm Ta film on trenches and vias etched on SiO_2. Trench width 130 nm, aspect ratio 7:1.

growth mode prevents any blocking of the trench entrance. Figure 11.38 shows a set of trenches filled with void-free copper under these conditions.

The same process was used to deposit highly conformal Ta films on trenches and vias etched on SiO_2. For instance, a duty cycle of 12.5% was used to deposit 10-, 20-, and 30-nm-thick Ta films with thickness variation better than 15% across the entire trench. Figure 11.39 shows the image of a 20-nm Ta film on trenches 130 nm wide and aspect ratio 7:1. The morphology of the film at the trench entrance shows no signs of overhang.

11.8 CONCLUSIONS

In order to assess the future of plasma immersion ion implantation and plasma immersion ion implantation and deposition (PIII&D) processes in the semiconductor industry, it is important to directly compare them with presently dominant techniques. First, we compare PIII with conventional beamline ion implantation. The following summary lists some of the advantages, disadvantages, and concerns of both conventional implantation and PIII.

1. **Conventional Beamline Ion Implantation**

Advantages: dose control, uniformity, repeatability, installed base, mass analysis, monoenergetic, tilt capability, versatility, and many doping steps.

Disadvantages/Concerns: high cost, large footprint, low dose rate at low energy, channeling, damage, charging, hard to cluster, contamination worse at low energy.

2. **Plasma Immersion Ion Implantation**

Advantages: high dose rate at low energy, cluster tool compatible, small footprint, conformal doping (less shadowing), and reduced charging.

Disadvantages/Concerns: no mass analysis, channeling, damage, inaccurate in situ dose measurement, and uniformity.

In this comparison, the desirable features of PIII include the ability to form ultrashallow junctions, low total cost, small size, and cluster tool compatibility. This burgeoning technology has been demonstrated to work well in many areas and may well be on its way to become the technique of choice in ultra-large-scale integration (ULSI) processing, particularly shallow junction and SOI formation.

Second, we compare MePIIID with other metallization approaches. MePIIID can be used for the complete copper metallization process, which includes the deposition of a conformal diffusion barrier *and* the complete filling of vias and trenches with copper. Alternatively, MePIIID can also be used for the deposition of the diffusion barrier followed by the deposition of a *conformal* copper seed layer, which is required if the final copper deposition is done by an electrochemical process. There are advantages in the first approach in terms of reduction of contamination: The entire process can be carried out without breaking vacuum or immersing the wafer in a liquid electrolyte. However, because electrochemical deposition has a high deposition rate, it is possible that the second approach will gain practical importance. Another argument for conventional electrolytic processes is that the industry is familiar and experienced with them, and their costs are relatively low. The reduction of hazardous waste as well as further extreme miniaturization are driving forces that may lead to MePIIID acceptance and application in the semiconductor industry.

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