Microstructure and crystallinity of porous silicon and epitaxial silicon layers fabricated on $p^+$ porous silicon

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Epitaxial silicon layers fabricated on porous silicon have many applications, and a recent one is the production of silicon-on-insulator substrates. In this work, the microstructure and crystallinity of $n^-$ (lightly doped, n-type), $n^+$ (heavily doped, n type), $p^-$ (lightly doped, p type), and $p^+$ (heavily doped, p type) porous silicon are systematically investigated by transmission electron microscopy and high-resolution x-ray diffraction. The results show that $p^+$ porous silicon has the best quality compared to $n^-$, $n^+$, and $p^-$ porous silicon and is the best substrate to fabricate epitaxial silicon. Non-uniform porosity is detected in $n^+$ porous silicon formed without exposure to light. Silicon epitaxial layers produced by ultrahigh vacuum electron evaporation on $p^+$ (100) porous silicon are consequently investigated. Our study shows that preoxidization of porous silicon before epitaxy is very important because it not only improves the crystal quality of the epitaxial layer but also prevents boron diffusion into the epitaxial layer during growth. © 2003 American Vacuum Society. [DOI: 10.1116/1.1537714]

I. INTRODUCTION

Porous silicon formed by electrochemical anodization of silicon in HF is used in silicon-based optoelectric devices such as light emitting devices, waveguides, photonic crystals, and solar cells. In addition, because of its high oxidation rate, porous silicon can be used to fabricate silicon-on-insulator (SOI) via the full isolation by porous oxidized silicon (FIPOS) process. Recently, an epitaxial layer transfer technique called ELTRAN is successful in fabricating SOI materials. The process makes use of the fragile nature and chemical properties of porous silicon. In this method, epitaxial silicon is fabricated on porous silicon and subsequently bonded to an oxidized silicon wafer. The bonded wafer is then split at the position of the porous silicon using a water jet, and the SOI structure is formed after the porous silicon is removed by etching. In both FIPOS and ELTRAN, the fabrication of an epitaxial layer on porous silicon is needed and a detailed understanding of the microstructure and other characteristics of the porous silicon and epitaxial thin film is very important. The knowledge is also beneficial to heteroepitaxial processes involving the synthesis of other materials such as SiGe, GaAs, and PbS on porous silicon.

X-ray diffraction (XRD) is an effective method to investigate the crystal quality. Many people have investigated $p$-type porous silicon by XRD and a few researchers have studied the crystallinity of $n$-type porous silicon. However, previous works have not been conducted systematically and many phenomena are still not well understood. In addition, although the effects of preoxidation on the microstructure of porous silicon have been investigated, those on the quality of epitaxial layers have not been studied. In this work described here, the crystallinity of four typical types of porous silicon was systematically studied by both transmission electron microscopy (TEM) and XRD. Based on these results, Si epitaxy on porous silicon was further investigated. The microstructure, crystallinity, surface topography, and electric properties of the epitaxial layer were characterized. Our results also show that preoxidation can prevent boron diffusion during the growth process.

II. EXPERIMENT

Porous silicon samples were produced by electrochemical anodization in an HF/ethanol electrolyte with equal concen-
trations at different current densities and for different time durations. Four types of (100) Si wafers were used: lightly phosphorus doped (1–3 Ω cm, \( n^- \)), heavily phosphorus doped (0.01–0.03 Ω cm, \( n^+ \)), lightly boron doped (1–3 Ω cm, \( p^- \)) and heavily boron doped (0.01–0.03 Ω cm, \( p^+ \)). Anodization was performed at room temperature and without light.

An ultrahigh vacuum electron beam evaporator (UMS 500P) was employed to grow epitaxial silicon on the porous silicon samples. One of the porous silicon samples was oxidized at 400 °C for 1 h in dry oxygen, whereas the other sample was not preoxidized. Prior to epitaxy, both samples were dipped in diluted HF for a short time to remove the thin surface oxide and then rinsed by de-ionized water before loading into the chamber. The base pressure in the chamber was \( 10^{-9} \) mbar and the temperature of the substrate was maintained at 850 °C during the epitaxial process.

High-resolution XRD was performed on a Philips X’pert equipped with a two-crystal four-reflection Ge [220] diffractometer. The Cu \( K\alpha_1 \) radiation with a wavelength of 1.5406 Å and fourfold Ge (220) reflection were monitored in our experiments. An \( \omega/2\theta \) scan was performed on the (004) plane. This technique is very sensitive to lattice displacement and strain in the direction perpendicular to the diffraction plane of the crystal.

Cross-sectional TEM was conducted to reveal the microstructure of the epitaxial layers and porous silicon. The surface morphology of the samples was assessed using atomic force microscopy (AFM), and the crystal quality of the epitaxial silicon was measured by Rutherford backscattering spectroscopy (RBS) and channeling using 2.0 MeV helium ions and a scattering angle of 170 °C.

III. RESULTS AND DISCUSSION

A. Microstructure and crystallinity of porous silicon

The doping type and concentration influence the structure of the porous silicon greatly. Figure 1 depicts the cross-sectional TEM (XTEM) pictures of the four types of porous silicon. In the porous silicon formed in \( n^- \) silicon shown in Fig. 1(a), the pores perpendicular to the surface are large (~0.5 μm) and the distance between the pores is about 1.5 μm. There are also many branches beside the column pores. In comparison, the pores in the \( n^+ \) porous silicon do not resemble columns but rather trees. The diameter of the pores is about 10 nm. Figures 1(b) and 1(c) exhibit the microstruc-
tures at shallow and deep positions, respectively, and the porosity at a larger depth is observed to be higher. Figure 1(d) shows the XTEM of $p^+$ porous silicon that resembles a sponge and it is difficult to discern individual pores. Therefore, the pore size is at most on the order of several nm. The structure of the $p^+$ porous silicon shown in Fig. 1(e) is similar to that of $n^+$, and the diameter of pores is about 10 nm.

High-resolution XRD is used to evaluate the crystallinity of the samples. Figure 2 shows the high-resolution XRD spectra acquired from the porous silicon. There are two peaks, one originating from the silicon substrate and the other from porous silicon. The porous silicon peak is on the left of the silicon peak, and so the lattice constant of the porous silicon perpendicular to the surface is larger than that of the substrate. For the $n^-$ porous silicon sample shown in Fig. 2(a), only the silicon substrate peak can be observed, but there is also a clear hump below it, implying that the porous silicon peak overlaps that of the substrate. Hence, the crystallinity of the $n^-$ porous silicon is the same as that of the silicon substrate and no obvious strain exists between them. On the other hand, two broad peaks consisting of several subpeaks appear from the $n^+$ porous silicon [Fig. 2(b)]. The observation is consistent with our TEM data as well as results by others. The $p^-$ porous silicon spectrum in Fig. 2(c) reveals that there is a bigger lattice mismatch (about 0.37%) between the porous silicon and substrate. The width of the peak is closely related to the degree of crystallinity. The peak width of $p^-$ porous silicon is close to that of the substrate. For $p^+$ porous silicon [Fig. 2(d)], the lattice mismatch between the porous silicon and substrate is quite small and about 0.05%. The width of the $p^+$ porous silicon peak from the sample formed using a small current density is only slightly larger than that of the silicon substrate. Therefore, it can be inferred that the $p^+$ porous silicon has good crystallinity and there is only a small strain between the porous silicon and substrate. A hump below the porous silicon peak can be observed due to scattering between the pores, and the width of the hump is related to the size of the pores. Our results disclose that the peak width decreases with higher anodizing current density.

The intrinsic causes for the expansion of porous silicon are still unknown. However, our results indicate that the crystallinity of porous silicon is closely related to its microstructure. The smaller the silicon column, the larger the strain. The TEM results disclose a big difference between $n^+$ and $n^-$ porous silicon. Holes are needed during the formation of porous silicon. In $p$-type silicon, holes are the majority carriers while the situation in $n$-type silicon is the opposite. The results of Memming show that the generation of holes in the surface layer of $n$-type silicon is due to breakdown. The interface between solution and silicon can be considered as a Schottky junction with a negative voltage. When the electric field strength is large enough, breakdown of the silicon occurs, and a large amount of electrons and holes will consequently be generated. The breakdown voltage is a function of the doping concentration, and decreases with higher doping level. Silicon breakdown occurs in the presence of an electric field in excess of $3 \times 10^5$ V/cm, and the electric field strength is a function of the bias, doping concentration, and geometry. A high doping concentration or sharp pore tips in the anode surface lowers the breakdown bias. Hence, breakdown cannot occur in $n^+$ type silicon in the initial stage because holes generated by thermal excitation are few in numbers. It is generally agreed that pits will

![Fig. 2. High-resolution XRD rocking curves acquired from: (a) $n^-$ porous silicon, (b) $n^+$ porous silicon, (c) $p^-$ porous silicon, and (d) $p^+$ porous silicon.](image-url)
initially form randomly on the surface and only pits with a curvature smaller than the critical radius can further dissolve due to the holes generated by breakdown. It has been shown that the density of the pore tips is determined by the space-charge region based on the Beale model\textsuperscript{16} or by the diffusion length according to the diffusion-limited aggregation model.\textsuperscript{17} Both the space-charge region and the diffusion length are related to the doping concentration and applied voltage. For \(n^-\) porous silicon, the space-charge region is large and therefore the distance between the pores is quite large. On the contrary, tunneling can occur in \(n^+\) silicon because of the high doping concentration and that many holes can be generated. Hence, the density of the pore tips is greater than that in \(n^-\) silicon.

Inhomogeneity is observed from the \(n^+\) porous silicon and our observation is consistent with the XRD results reported by Chamard and Dolino.\textsuperscript{12} Takemoto \textit{et al.}\textsuperscript{13} have suggested the following. (a) When a highly doped \(n\)-type silicon is anodized for a long reaction time, the resultant porous silicon layer exhibit multilayered pore structures depending on the distance from the surface. (b) The pore morphology, pore diameter, and distance between pores change significantly with the current density. The higher the current density, the simpler the pore structure and the larger the pore diameter. Lehman \textit{et al.}\textsuperscript{18} have also observed inhomogeneity in \(n\)-type silicon. An increase in the pore diameter and porosity with depth is observed, and it is thought to be due to the reduced electrolyte concentration with pore depth as a result of limited diffusion in the narrow bottleneck region. However, the non-uniformity is not observed in \(p\)-type silicon, including in \(p^-\) porous silicon with smaller pores. Based on the XTEM results, the diameter and density of the pores in \(n^+\) porous silicon and \(p^+\) porous silicon are similar. Therefore, in addition to the reduction in the electrolyte concentration, there appear to be other mechanisms.

The XTEM and XRD data suggest that \(p^+\) porous silicon is the best material for epitaxy. It maintains good crystallinity, has a small lattice mismatch with bulk silicon, and it is suitable for epitaxy. On the other hand, although the crystallinity of \(n^-\) porous silicon is fine, the pores are too big.

**B. Epitaxy of Si on \(p^+\) (100) porous silicon by ultrahigh vacuum electron beam deposition**

The common techniques to fabricate silicon epitaxial layers are molecular beam epitaxy (MBE) and chemical vapor deposition (CVD). MBE is a good method to grow high-quality epitaxial layers because of its low growth rate and accurate control, but the cost is high. CVD is widely used in the integrated circuit industry, but the growing temperature, however, is so high that the porous silicon will be destroyed. In this work, an alternative method, ultrahigh vacuum electron beam deposition, is employed. The deposition temperature is about 850 °C at which the structure of the preoxidized porous silicon is still stable. As our aforementioned experiments suggest that \(p^+\) porous silicon is the best for silicon epitaxy, we have only produced silicon epitaxial layers on \(p^+\) porous silicon for the following studies.

Figures 3(a) and 3(b) show the structure of the silicon epitaxial layer on preoxidized porous silicon and on the porous silicon substrate without preoxidization, respectively. No extended defects are observed in the epitaxial layer on the preoxidized porous silicon, whereas many defects exist in the other one. The interface shown in Fig. 3(a) is normal between porous silicon and the epitaxial layer. The main defects in Fig. 3(b) are stacking faults and most of them originate from the surface of the substrate along the \{111\} planes.

AFM measurements (not shown here) show that when the epitaxial film is thin, the surface is rough and there are many shallow pits, but on the other hand, if the film is thick, the surface is very smooth. Contrary to bulk silicon, the porous silicon has many pores on the surface. It has been shown that at the initial growth stage, the pores are effective sinks for adatoms, and therefore the pore filling will occur at first thereby impeding the growth on the surface.\textsuperscript{19} Our results propose the following mechanism. When the pores are small enough, the islands will grow on the surface of the substrate, and so the surface becomes rough. After the islands merge with each other, the surface will become smooth again. Subsequent growth is layer by layer.

Herino \textit{et al.}\textsuperscript{18} showed that the structure of as-prepared porous silicon changes at high temperature but preoxidation can prevent it. During silicon epitaxy, the pores in the porous silicon without preoxidization enlarge, and then the pores cannot be filled sufficiently. The \{111\} planes have the
highest areal density and they are also the selective growth plane for epitaxy. Si on the side of the pores will grow along \{111\}, and stacking faults form when the three-dimensional islands are translated relative to each other by a non-lattice vector.

The RBS spectra shown in Fig. 4 disclose the crystallinity of the two epitaxial layers. The quality of the thin film grown on the pre-oxidized substrate is very good and close to the perfect crystal. However, the channeling yield at the interface of the just prepared sample is high due to high defects. Hence, preoxidization is very important to high quality epitaxy.

Figure 5 shows the high-resolution XRD spectrum of the epitaxy silicon layer on porous silicon. Two porous silicon peaks are found. The left one is the preoxidized porous silicon and the right one is the porous silicon whose oxides have been removed before epitaxy. The epitaxial layer is not observed since it is too thin. The lattice constant of the porous silicon is large and different from the result of CVD epitaxial growth.\(^\text{20}\) We have investigated the strain in epitaxial GeSi on the same porous silicon. In the spectrum acquired from the as-prepared sample at 700 °C, the position of the porous silicon peak is to the left of the substrate peak, but the position changes to the right after the sample has been annealed at 800 and 1000 °C. Considering independent results acquired from Si and GeSi, it can be inferred that the strain in porous silicon is related to both temperature and the epitaxial layer. The CVD growth temperature is higher than that used in ultrahigh vacuum electron beam evaporation and changes the strain in the porous silicon.

Borod diffusion may play an important role since the porous silicon substrate is heavily boron doped. Figure 6 displays the spreading resistance profiles (SRP) of the epitaxial layer on: (a) preoxidized porous silicon and (b) as-prepared porous silicon. The insets are magnified figures.

IV. CONCLUSION

The crystallinity of \(n^-\) porous silicon is the same as that of the substrate because of its large pore-to-pore distance.
Non-uniform porosity is found in $n^+$ porous silicon, but not the other three types. Compared with other porous silicon types, there is a bigger lattice mismatch between $p^-$ porous silicon and the silicon substrate. According to the microstructure and crystallinity revealed in this study, the porous silicon formed on $p^+$ silicon is the best material for subsequent Si epitaxy. The quality of the epitaxial layer grown on preoxidized porous silicon is good, but many stacking faults along the $\{111\}$ direction are found in the epitaxial layer on unoxidized porous silicon. The oxide formed on the surface of porous silicon appears to prevent boron diffusion into the epitaxial layer during the growth.

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