Formation of silicon on plasma synthesized $\text{SiO}_x\text{N}_y$ and reaction mechanism

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Abstract

The application of silicon-on-insulator (SOI) substrates to high-power integrated circuits is hampered by self-heating effects due to the poor thermal conductivity of the buried SiO$_2$ layer. We propose to replace the buried SiO$_2$ layer in SOI with a plasma synthesized SiO$_x$N$_y$ thin film to mitigate the self-heating effects. The SiO$_x$N$_y$ films synthesized on silicon by plasma immersion ion implantation (PIII) exhibit outstanding surface topography, and excellent insulating characteristics are maintained up to an annealing temperature of 1100 °C. Hence, the polycrystallization in our SiO$_x$N$_y$ materials is insignificant during conventional complementary metal oxide silicon (CMOS) processing. Using Si/SiO$_x$N$_y$ direct bonding and the hydrogen-induced layer transfer, a silicon-on-SiO$_x$N$_y$ structure has been successfully fabricated. Cross-sectional high-resolution transmission electron microscopy (HRTEM) and spreading resistance profiling (SRP) reveal that the bonded interface is abrupt and the top Si layer exhibits nearly perfect single crystalline quality. The reaction mechanism of SiO$_x$N$_y$ and Si wafer bonding are also discussed.

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1. Introduction

Silicon-on-insulator (SOI) offers many inherent benefits over bulk silicon substrates for high speed, low-power complementary metal oxide semiconductor (CMOS) integrated circuits. Advantages include
low parasitic capacitance, radiation hardness, high packing density, absence of latch-up, and compatible fabrication processes [1–3]. Hence, it has become the substrate of choice for a number of sub-micrometer microelectronic devices. However, the use of the SOI in high-power integrated circuits is hampered by the self-heating effects caused by the poor thermal conductivity of the insulating SiO₂ layer that is approximately 100 times worse than that of silicon [4]. Moreover, as the device geometries shrink and transconductance as well as current density increase with MOS scaling, the self-heating effects will become more pronounced. Hence, in order to develop integrated circuits with on-chip power devices, it is important to investigate an alternative buried insulator with better thermal conductivity [5].

One of the interesting buried insulators is silicon nitride (Si₃N₄) with a thermal conductivity about 20 times higher than that of SiO₂ (30 W/m K versus 1.4 W/m K). The Si/Si₃N₄/Si and Si/SiO₂/Si₃N₄/Si structures have been studied [6] and these new structures exhibit much better thermal performance than conventional SOI with a buried oxide layer [7]. Thus, the use of Si₃N₄ as the buried insulator in SOI is a good alternative from the standpoint of the mitigation of the self-heating effects. SOI structures with buried nitride can be synthesized by conventional beam-line high-dose nitrogen ion implantation into silicon [8], but this process is quite expensive due to the long implantation time to attain the high nitrogen dose that ranges from 10¹⁷ to over 10¹⁸ atoms/cm². Alternatively, synthesis of silicon-on-nitride by the wafer bonding method has been reported [9]. In this method, the Si₃N₄ layer was fabricated using chemical vapor deposition (CVD) that was quite complicated and also expensive. Even though a Si₃N₄ layer can be synthesized by several techniques, plasma immersion ion implantation (PIII) has an edge in a number of aspects and is an emerging technology particularly for high-dose rate implantation due to its high efficacy [10,11]. In PIII, the sample is immersed in a plasma shroud from which ions are extracted and accelerated across the plasma sheath into the wafer. The dose rate can be as high as 10¹⁶ ions/cm² s, which is equivalent to 10 monolayers of implanted atoms per second and at least an order of magnitude higher than that of a conventional ion implanter. In addition, the implantation time is independent of wafer size and this bodes well for 300 mm wafer processing. Therefore, the synthesis of the Si₃N₄ layer by PIII is quite attractive. However, it is known that polycrystallization occurs in buried Si₃N₄ layers during annealing leading to a leaky dielectric [12]. In contrast, a silicon oxynitride (SiOₓNᵧ) buried layer does not crystallize even after high temperature annealing [13]. Moreover, a SiOₓNᵧ layer with the optimal composition should incorporate the positive features of SiO₂ and Si₃N₄ such as resistance against radiation hardening [14].

In this work, we synthesized thin surface layers of silicon oxynitride (SiOₓNᵧ) by conducting sequential nitrogen and oxygen PIII into silicon. The surface morphology and chemical composition of the films were investigated. The wafers with the SiOₓNᵧ surface layers were subsequently bonded to hydrogen-implanted donor wafers at room temperature a Si/SiOₓNᵧ/Si structure was produced using the ion-cutting method. The substrates were characterized using chemical and electrical techniques confirming success of the fabrication. The reaction mechanism of SiOₓNᵧ and Si wafer bonding are also discussed.

2. Experimental

2.1. SiOₓNᵧ synthesis by PIII

100 mm diameter p-type Si(1 0 0) wafers with resistivity of 10–20 Ω cm were loaded into vacuum chamber and treated in our PIII facility [15]. Prior to PIII, the main vacuum chamber was pumped to a base pressure of 6 × 10⁻⁶ Torr and then the samples were cleaned using argon ion sputtering for 15 min. High purity nitrogen and oxygen gases were subsequently bled into the chamber sequentially. The nitrogen and oxygen PIII durations were 4 and 2 h, respectively. The working pressure was maintained at 8 × 10⁻⁴ Torr, and the plasma was generated by a radio frequency inductive coupled plasma source (RF-ICP) operated at an input power of 1000 W. The plasma density in the vacuum chamber was monitored using a Langmuir probe and in our previous studies [16], the plasma density was measured to vary less than 10% within a 600 mm diameter in the vacuum chamber and the electron temperature was in the range of 3–4 eV. During the experiments, a tetrode-based pulse mod-
ulator was used to produce short square high-voltage pulses. A Pearson model 305A voltage divider, Pearson model 3525 current monitor, and Tektronix 460A digital oscilloscope were employed to measure the applied voltage and the output current. The potential applied to the backside of the sample was $-30 \text{kV}$ with a pulse width of $30 \text{ ms}$ and repetition rate of $200 \text{ Hz}$.

The nitrogen and oxygen implant doses are estimated to be about $2 \times 10^{17}$ and $1 \times 10^{17} \text{ cm}^{-2}$, respectively, based on similar experiments conducted in the same instrument and the voltage–current waveforms. After PIII, portion of the samples were annealed at $1100 \text{ °C}$ in nitrogen ambient with about $1\%$ oxygen (contamination due to minor leakage in our furnace determined from previous experiments). To determine the properties of the samples, techniques such as atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS), and X-ray diffraction (XRD) were employed.

2.2. \textit{Si/SiO}_x\textit{N}_y/\textit{Si} structure formation

After PIII, the SiO$_x$N$_y$-covered-Si wafer was bonded to a Si donor wafer that had been previously implanted with hydrogen ($50 \text{ kV}$ and $6 \times 10^{16} \text{ cm}^{-2}$) to form the Si/SiO$_x$N$_y$/Si structure. Before bonding, both wafers were cleaned with a H$_2$SO$_4$:H$_2$O$_2$ (10:1) solvent at $120 \text{ °C}$ for $10 \text{ min}$, followed by rinsing in de-ionized (DI) water and spin drying. The surfaces
were then activated in a 400 W oxygen plasma (oxygen pressure of 1.3 Torr) at 100 °C for 60 s. After activation, they were dipped in a modified RCA-1 solution \((\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:6:30)\) at 70–75 °C for 60 s, followed by rinsing in DI water and spin drying again. Afterwards, the two wafers were placed with the mirror surfaces facing each other separated by three removable spacers in air at room temperature. Direct bonding occurred over the entire surface of the wafers within seconds under a small applied pressure at the center by tweezers after removing the spacers. After bonding, the pair was heated to 120 °C for 2 h in air, and then temperature was raised to 200 °C for another 10 h to improve the bonding strength. Subsequently, the bonded wafer was furnace annealed at 300 °C for 2 h under nitrogen and the temperature was finally raised to 450 °C for 10–15 min to induce splitting of the thin Si layer to complete the transfer of a thin silicon layer onto the SiO\(_x\)N\(_y\)-covered-silicon wafer. The resulting Si/SiO\(_x\)N\(_y\)/Si structure was

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**Fig. 3.** (a) TEM micrograph of the Si/SiO\(_x\)N\(_y\)/Si structure formed using direct wafer bonding and hydrogen-induced layer transfer. (b) HRTEM micrograph of the buried SiO\(_x\)N\(_y\) layer showing the double layer structure. (c) HRTEM micrograph of the interfacial region between the top Si layer and buried SiO\(_x\)N\(_y\) layer indicating a defect-free and single crystal Si layer as well as an abrupt bonded interface. The bottom interface between SiO\(_x\)N\(_y\) layer and Si substrate is coarser than the upper interface shown in (c).
investigated by high-resolution transmission electron microscopy (HRTEM) and spreading resistance (SPR) to confirm the successful formation of SOI structure.

3. Results and discussion

3.1. Characterization of SiO$_x$N$_y$ surface layer

The objective of our work is to fabricate Si/SiO$_x$N$_y$/Si structure using the ion-cut process. In this process, whether or not bonding is successful is mostly determined by the low surface roughness of the SiO$_x$N$_y$ film. Therefore, AFM was performed initially to examine the surface morphology of the as-implanted sample, and the three-dimensional AFM image is depicted in Fig. 1. It can be observed that the surface of the SiO$_x$N$_y$ is smooth and uniform with a root-mean-square (RMS) roughness value of 0.162 nm that is good enough for direct bonding obviating the needs for complicated lapping and polishing procedures. XPS was performed to determine the elemental depth profiles in the annealed SiO$_x$N$_y$ thin film. The 1100 °C as-annealed sample was analyzed using a PHI 5802 X-ray photoelectron spectrometer with a monochromatic Al Kα source. Fig. 2 shows the corresponding depth profiles of N, O and Si. It is obvious that two layers can be found. From the surface to a depth of around 40 nm, the amounts of O and N are about 40% and 20%, respectively. From 40 nm onwards, the O concentration diminishes gradually but that of N increases compared to the first layer. The higher structural disorder confirmed by XRD analysis (not shown here) in the SiO$_x$N$_y$ film after annealing at 1100 °C can be attributed to the presence of O. This should help prohibit polycrystallization of the buried insulator during post annealing in conventional CMOS processes.

3.2. Characterization of the Si/SiO$_x$N$_y$/Si structure

In order to examine the quality of the bonded interfaces in the Si/SiO$_x$N$_y$/Si structure, transmission electron microscopy (TEM) was employed. Fig. 3(a) depicts the micrograph of the bonded structure showing direct evidence of the formation of the Si/ SiO$_x$N$_y$/Si structure. The thicknesses of top Si layer and buried SiO$_x$N$_y$ layer are about 400–450 and 80 nm, respectively. The damaged surface region can be easily etched away and the top silicon layer can be further reduced to the desirable thickness by dry etching. Fig. 3(b) displays the high-resolution TEM image of the buried SiO$_x$N$_y$ layer, which obviously reveals the double layer structure. The thicknesses of these two layers are about 43 and 33 nm, respectively, and are consistent with our XPS results. A possible explanation is as follows. In our experiments, nitrogen and oxygen were sequentially implanted into Si. Before O implantation, the sub-surface region in the substrate has transformed into SiN$_x$. It is known that the O projected range in SiN$_x$ is shorter than that in Si because the density of SiN$_x$ is larger but the O and N projected ranges in Si are similar. Hence, in our SiO$_x$N$_y$ film, the O in-depth distribution is narrower than that of N resulting in the formation of two layers after high temperature annealing. The layer close to the top Si has a higher O concentration than that of close to Si substrate. Our high-resolution TEM image reveals the interfacial region between the top Si layer and SiO$_x$N$_y$ buried layer (upper interface, shown in Fig. 3(c)). It can be observed that the upper interface is as sharp as a few atomic layers. The SiO$_x$N$_y$ layer is homogeneous and amorphous, and the Si atoms are well aligned without showing any observable structural defects. Our results clearly indicate that our process is capable of producing nearly perfect single crystal top Si on a SiO$_x$N$_y$ buried layer.

![Fig. 4. Spreading resistance profile of the Si/SiO$_x$N$_y$/Si structure clearly showing the three-layered structure with very steep interfaces.](image-url)
SRP was employed to study the electrical property of the Si/SiO\textsubscript{x}N\textsubscript{y}/Si structure and the resulting depth profile is shown in Fig. 4. Three layers including the top silicon layer, buried SiO\textsubscript{x}N\textsubscript{y} layer and Si substrate can be distinguished clearly with very steep interfaces. The very steep slope from the top silicon to buried SiO\textsubscript{x}N\textsubscript{y} at a depth of 430 nm in the spreading resistance profile implies a sharp interface between them. The spreading resistance values obtained show that the top silicon has uniform conductivity and the buried SiO\textsubscript{x}N\textsubscript{y} layer exhibits excellent insulating characteristics. The thicknesses of the top silicon and buried SiO\textsubscript{x}N\textsubscript{y} are in also agreement with the HRTEM results.

3.3. Reaction mechanism of SiO\textsubscript{x}N\textsubscript{y} and Si wafer bonding

It is known that the bonding energy associated with wafer bonding at room temperature is too low and a subsequent heating step is necessary to induce chemical reactions at the interface leading to a higher bonding energy. The significant difference in the activation energy between Si\textsubscript{3}N\textsubscript{4} direct bonding [17] and silicon direct bonding would suggest that a considerably different surface chemistry is involved in the Si\textsubscript{3}N\textsubscript{4} bonding process compared to that of Si direct bonding. The final stage of the cohesive bond in

Fig. 5. Infrared transmission picture of a bonded pair after the crack-opening test: (a) as-bonded, (b) after annealing at 120 °C, (c) after annealing at 300 °C.
speculate a chemical reaction as follows:

\[ \text{Si}-(\text{O}_x\text{N}_y)\text{–H} + \text{Si–OH} \rightarrow \text{Si}-(\text{O}_x\text{N}_y)\text{–Si} + \text{H}_2\text{O} \]  

(1)

The reaction starts to form strong Si–(O_xN_y)–Si covalent bonds across the bonding interface at temperature about 120 °C. In our wafer cleavage process, the crack-opening method [18] was used by inserting a 0.05 mm thick razor blade between the bonded pair from the beveled edge on one side. The resulting equilibrium crack length was measured using an infrared transmission imaging system to estimate the bonding strength. Fig. 5(a) and (b) depicts the infrared transmission photos of as-bonded pair and as-annealed pair, respectively. It is obvious that the bond strength has been improved significantly after 120 °C annealing. For the sample annealed at 300 °C for 2 h, the bond strength was sufficiently strong to withstand exfoliation, and the infrared transmission photo was shown in Fig. 5(c). During theses heating steps, molecular water formed in reaction (1) will oxidize the surrounding crystalline silicon and form molecular hydrogen via the reaction:

\[ \text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2 \]  

(2)

The released hydrogen is most likely absorbed by the amorphous SiO_xN_y layer. Molecular hydrogen and high internal gas pressure at the bonding interface may therefore be avoided resulting in bubble-free bonding interface and high-quality SOI materials with SiO_xN_y as the buried layer.

4. Conclusion

In summary, we have successfully produced high-quality and heat-resistant silicon-on-SiO_xN_y materials using direct wafer bonding and H-induced layer transfer method. The SiO_xN_y films synthesized by our PIII process exhibit outstanding surface topography and maintain amorphous structure up to an annealing temperature of 1100 °C. This bodes well for post annealing in CMOS processing. The HRTEM and SPR results confirm the formation of the SOI structure and also show that the bonded interface is sharp and the top Si layer has almost perfect crystal quality.

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