Germanium movement mechanism in SiGe-on-insulator fabricated by modified Ge condensation

Zengfeng Di\textsuperscript{a} and Paul K. Chu\textsuperscript{b,1}\textsuperscript{1}

Department of Physics and Material Science, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong, China

Miao Zhang, Weili Liu, Zhitang Song, and Chenglu Lin

The Research Center of Semiconductor Functional Film Engineering Technology and State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology (SIMIT), Chinese Academy of Sciences (CAS), Shanghai 200050, People’s Republic of China

(Received 7 October 2004; accepted 14 December 2004; published online 11 March 2005)

The movement of Ge during Ge condensation in SiGe-on-insulator (SGOI) fabrication is studied based on the competition between the diffusion of Ge atoms and accumulation of Ge atoms. The diffusion of Ge atoms overwhelms the Ge accumulation at the top thermal oxide/SiGe interface, resulting in a flat Ge profile in the SGOI layer. However, the opposite result is found at the bottom SiGe/buried-oxide (BOX) interface. The Ge diffusion towards the BOX is blocked because of the much smaller diffusion coefficient of Ge in the BOX than that in the SiGe layer. The Ge accumulation effects are more dominant than the diffusion of Ge, and so Ge atoms pile up near the BOX giving rise to an abrupt profile. The disappearance of the SiGe lattice structure near the SiGe/BOX interface is also found in the sample oxidized for a longer time due to the reduction of the melting point of SiGe alloys with higher Ge fractions. © 2005 American Institute of Physics. [DOI: 10.1063/1.1857060]

I. INTRODUCTION

Strained Si with in-plane tensile strain is a promising material for high-performance metal-oxide-semiconductor field-effect transistors (MOSFETs) due to enhanced carrier mobilities.\textsuperscript{1,2} In addition, multichannel structures with compressively strained SiGe layers and tensilely strained Si exhibit symmetrical mobility enhancements for both electrons and holes, making them attractive for next-generation complementary metal-oxide-semiconductor (CMOS) technology.\textsuperscript{3,4} Similarly, the incorporation of silicon-on-insulator (SOI) into CMOS technologies gives rise to advantages such as reduced parasitic capacitance, increased circuit density due to tighter isolation, and reduced short-channel effects as well as latch-up.\textsuperscript{5} Combination of strained Si layers with SOI formed by epitaxial growth of strained Si layers on relaxed SiGe-on-insulator (SGOI) substrate harnesses both benefits and has recently attracted much attention from the microelectronics industry.

In order to scale down strained SOI MOSFETs while retaining high performance and reliability, fabrication of high-quality SGOI substrates is of paramount importance. Attempts have been made to fabricate SGOI substrates. Huang et al.\textsuperscript{6} and Brunner et al.\textsuperscript{7} utilized an ultrathin SOI as a “compliant substrate” to partially relax an initially strained SiGe film.\textsuperscript{6,7} An et al.\textsuperscript{8} and Mizuno et al.\textsuperscript{9} carried out separation by implantation of oxygen (SIMOX) on a strained-relaxed SiGe virtual substrate.\textsuperscript{8,9} Huang et al.\textsuperscript{10} used the Smart-Cut\textsuperscript{TM} technique to transfer a layer of SiGe onto the oxide. However, most SGOI layers fabricated by these methods do not meet the application requirements as they are too thick and/or have a too low Ge fraction. Recently, Tezuka et al.\textsuperscript{11} proposed a SGOI fabrication technology based on Ge condensation by oxidation of SiGe on a SOI layer. This technique is quite promising with respect to the fabrication of thin SGOI layers for fully depleted (FD) MOSFETs compared to other methods.\textsuperscript{12} The top semiconductor is very thin in FD MOSFETs, and so the semiconductor/buried-oxide (BOX) interface affects the FD device performance. Even though a poor interface is known to significantly degrade the FD device performance in SOI, the characteristics of the SiGe/BOX interface have not been examined thoroughly.

In this work, we study the movement and distribution of Ge atoms, particularly at the two oxide/SiGe interfaces, during SGOI fabrication by the modified high-temperature oxidation and Ge-condensation technique. Competition between Ge accumulation and diffusion is observed at the two oxide/SiGe interfaces leading to a desirable flatter Ge profile in the SiGe layer as well as an undesirable abrupt Ge profile near the bottom SiGe/BOX interface of the SGOI substrate.

II. EXPERIMENT

SGOI substrates were fabricated by oxidation of a sandwiched structure of Si/SiGe/Si. The SiGe layer with a uniform Ge composition of 18% was pseudomorphically grown on the ultrathin SOI substrate using SiH\textsubscript{4} and GeH\textsubscript{4} precursors. In order to avoid the formation of GeO\textsubscript{x} mixed (Si,Ge)O\textsubscript{2}, or SiO\textsubscript{2}–GeO\textsubscript{2} during the subsequent process, GeH\textsubscript{4} was shut off and an added Si cap about 20 nm thick was produced on the SiGe layer in our modified Ge-condensation technique. The samples were oxidized for 1...
and 2 h at 1150 °C in 100% oxygen ambient. The elemental depth profiles were determined by secondary-ion-mass spectroscopy (SIMS), and the structures and crystalline quality were assessed using transmission electron microscopy (TEM) and high-resolution x-ray diffraction (XRD).

III. RESULTS

Figures 1(a) and 1(c) show the elemental depth profile acquired from the samples oxidized at 1150 °C for 1 and 2 h acquired using a CAMECA IMS-6F, respectively. Good SiO₂/SiGe/SiO₂ demarcation is revealed in both samples. The elemental depth profiles in the surface oxide and BOX are uniform and continuous, and very little difference can be observed between them, indicating that no Ge oxide is embedded in the surface region. The entire Ge distribution is seen to move away from the oxide into the SiGe layer of the SGOI substrate. Figures 1(b) and 1(d) plot the Ge and Si relative distributions in the SiGe layer of each sample. A small gradient of the Ge profile is observed near the top thermal SiO₂/SiGe interface after thermal oxidation for a short time. The Ge gradient becomes a little higher as the oxidation time increases. Ge pileups at the SiGe/BOX interfaces can be observed in both samples and this unusual phenomenon becomes more prominent in the sample oxidized for a longer time.

Figures 2(a) and 2(b) display the cross-sectional TEM images of the samples oxidized for 1 and 2 h, respectively. The thickness of the SiGe layer is 94 and 54 nm in the sample after 1- and 2-h oxidation, respectively. The clear lattice images in both samples indicate that the rejected Ge atoms from the SiGe-oxide layer are located at the lattice points and no threading dislocation appears. However, the lattice becomes vague and only the outline of the lattice is observed at the SiGe/BOX interface, as shown in the layer labeled 3 in Fig. 2(a). This phenomenon becomes more severe when the oxidation time increases. In the layer labeled 6 in Fig. 2(b), the lattice structure near the SiGe/BOX of the 2-h oxidized sample disappears completely. The changes can be attributed to the pileup of Ge as seen in the SIMS results because the same interface in the original SOI substrate exhibits good quality.

Figure 3 compares the high-resolution XRD results acquired from the following samples: (a) no oxidation but annealed at 1000 °C for 20 min, (b) 1-h oxidation at 1150 °C,
and (c) 2-h oxidation at 1150 °C. The as-deposited sample was annealed at 1000 °C to relax the strain in the SiGe layer. In Fig. 3(a), the narrow diffraction peak located at 34.18° indicates that the as-deposited SiGe layer with 18% Ge is relaxed and has good crystal quality. For the 1-h oxidized sample shown in Fig. 3(b), due to a small gradient of the Ge profile and the presence of the Ge pileup at the SiGe/BOX interface, the SiGe peak is a little broader than that of the sample without oxidation. However, the peak location does not change because the sample after 1-h oxidation has the same thickness as the sample without oxidation (as shown in the TEM images) and they have the same Ge concentration. The entire Ge distribution is contained in the SiGe layer and Ge loss has been effectively suppressed. After oxidation for 2 h, a much broader SiGe peak results indicating that a steeper Ge gradient and more substantial Ge pileup at the SiGe/BOX interface as the oxidation time becomes longer. The SiGe peak is observed to move away from the Si peak due to the long oxidation time and a higher Ge composition in the SiGe layer.

IV. DISCUSSION

A schematic of the Ge atom movement during oxidation is displayed in Figs. 4(a)–4(d). There have been several reports concerning the effects of the preferential oxidation of Si over Ge in SiGe based on the larger negative Gibbs free energy to form SiO₂ compared to GeO₂.¹⁴ The standard Gibbs free energies of formation (ΔfG°) at 298.15 K for SiO₂ and GeO₂ are −856.3 and −521.4 KJ mol⁻¹, respectively.¹⁵ Neglecting the small temperature influence on
the Gibbs free-energy change ($\Delta G$), the reaction $\text{GeO}_2(\text{cr}) + \text{Si}(\text{cr}) \rightarrow \text{SiO}_2(\text{cr}) + \text{Ge}(\text{cr})$ should introduce a large negative change within the temperature range used in this work. Based on thermodynamics, Si is more reactive than Ge. Therefore, Ge atoms are rejected from the SiGe-oxide layer, and they accumulate at the top thermal oxide/SiGe interface after high-temperature oxidation. At the same time, the accumulated Ge atoms diffuse toward the substrate. This leads to a smeared interface between the SiGe and initial Si layer of the SOI, resulting in the conversion of the entire Si layer into SiGe, as shown in Fig. 4(b). As the Ge atoms reach the BOX layer, such diffusion is blocked abruptly because of much lower diffusion coefficient of Ge in SiO$_2$. Ge atoms consequently accumulate at the bottom SiGe/BOX interface, as shown in Fig. 4(c). Finally, a small Ge profile gradient and Ge pileup at the SiGe/BOX interface is achieved [Fig. 4(d)].

Following this proposed mode of Ge movement, we conclude that the competition between Ge diffusion and accumulation at the top SiO$_2$/SiGe interface and the bottom SiGe/BOX interface is very significant. Sugiyama et al.\textsuperscript{16} have already explained the first competition at the top SiO$_2$/SiGe interface from the point of view of the activation energy. Ge diffusion in Si has much higher activation energy than oxygen diffusion in SiO$_2$ and therefore, the temperature dependence of Ge diffusion is stronger than that of oxygen diffusion in SiO$_2$, which is the key factor affecting the accumulation rate of Ge atoms at the SiO$_2$/SiGe interface. As a result, Ge diffusion is more enhanced at high temperature than Ge accumulation leading to a flat Ge profile.

Contrary to the flat Ge profile at the top SiO$_2$/SiGe interface, Ge pileup at the bottom SiGe/BOX interface is observed. It is also a result of the competition between Ge diffusion and accumulation. As oxidation proceeds, the rejected Ge atoms diffuse towards the substrate sequentially, but diffusion is blocked abruptly due to the much lower diffusion coefficient of Ge in SiO$_2$. At the bottom SiGe/BOX interface, the diffusion rate of Ge decreases whereas the accumulation rate of Ge is not affected due to the continuous arrival of Ge atoms. Consequently, the arriving Ge atoms pile up at the SiGe/BOX interface. This phenomenon becomes more pronounced if the oxidation time is longer. The melting point of SiGe with a high Ge concentration is lower,\textsuperscript{17} as indicated by the Si–Ge alloy phase diagram in Fig. 5. In the sample oxidized for 2 h, the melting point of the SGOI layer with 34% Ge (marked in Fig. 5) decreases to 1184 °C [Ge concentration is determined by energy-dispersive x-ray spectrometry or energy-dispersive spectroscopy (EDS)]. At the bottom SiGe/BOX interface, the Ge concentration is higher than 34% because of the Ge pileup, and so the melting point of the SiGe layer must be reduced to near the oxidation temperature (1150 °C). Consequently, SiGe near the SiGe/BOX changes to a liquid phase at this oxidation temperature and the lattice structure of the SiGe layer near the SiGe/BOX is disrupted completely, as demonstrated by the TEM image. On the other hand, the Ge concentration of the sample oxidized for 1 h is 18%, and so the melting point of the SiGe layer near the BOX remains much higher than the oxidation temperature. No phase transition thus occurs during oxidation at 1150 °C and the lattice structure is partially retained. Slight disordering of the lattice appears just because of the abrupt Ge profile. All in all, our results demonstrate that the oxidation time should be optimized for individual oxidation temperatures in SGOI fabrication.

V. CONCLUSION

The competition between Ge diffusion and accumulation is significant leading to different effects at the top SiO$_2$/SiGe interface and the bottom SiGe/BOX interface. At the top interface, Ge diffusion is more dominant resulting in a flat Ge profile, whereas at the bottom interface, diffusion is blocked due to the much lower diffusion coefficient of Ge in the BOX. Ge accumulation predominates over diffusion thereby giving rise to Ge pileup at the SiGe/BOX interface. If the oxidation time is long, the lattice structure of the SiGe in the vicinity of the SiGe/BOX will be destroyed due to the lower melting point of SiGe with higher Ge concentrations.

ACKNOWLEDGMENTS

This work was jointly supported by the Hong Kong Research Grants Council (RGC) Competitive Earmarked Research Grant (CERG) No. CityU 1137/03E, City University of Hong Kong Strategic Research Grant (SRG) No. 7001642, Shanghai Rising-star Program No. 04QMX1463, the Special Funds for Major State Basic Research Projects Grant No. G2000036506, and the National Natural Science Foundation of China under Grant No. 90101012.