Thermal annealing effects on the structure and electrical properties of Al$_2$O$_3$ gate dielectrics on fully depleted SiGe on insulator

Zengfeng Di, a) Miao Zhang, Weili Liu, Qinwo Shen, Suhua Luo,a) Zhiting Song, and Chenglu Lin
The Research Center of Semiconductor Functional Film Engineering Technology, Shanghai Institute of Microsystem and Information Technology (SIMIT), Chinese Academy of Sciences (CAS), Shanghai 200050, People’s Republic of China and State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology (SIMIT), Chinese Academy of Sciences (CAS), Shanghai 200050, People’s Republic of China

Paul K. Chu
Department of Physics and Material Science, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong, China.

(Received 16 August 2005; accepted 1 March 2006; published 21 April 2006)

The interfacial characteristics and electrical properties of as-deposited and annealed Al$_2$O$_3$ gate dielectric films fabricated on fully depleted SiGe on insulator are investigated. The surface morphology of the gate dielectric is observed by atomic force microscopy, and its physical thickness and structure are determined by high-resolution transmission electron microscopy. Assessment of the energy shifts of the interfacial components observed by high-resolution x-ray photoelectron spectroscopy shows that oxidation of Ge occurs readily at the growth temperature, leading to a mixture of Si and Ge oxides at the Al$_2$O$_3$/SiGe interface. After annealing, the relative intensity of GeO$_2$, diminishes significantly, whereas the relative intensity of the Si suboxides or SiO$_2$ increases, and especially, the formation of silicate is observed. The chemical state changes in the interfacial layer affect the flatband voltage ($V_{fb}$) and the density of the interfacial states. © 2006 American Vacuum Society. [DOI: 10.1116/1.2190657]

I. INTRODUCTION

As the density of transistors increases on a chip, the dimensions of metal-oxide-semiconductor field effect transistors (MOSFETs) decrease correspondingly to meet the requirements of the International Technology Roadmap for Semiconductors (ITRS). Following the scaling rule, conventional Si base complementary metal-oxide-semiconductor (CMOS) transistors are quickly approached fundamental limits, and therefore, innovative device structures and materials must be considered to meet the expanding needs of the information technology. Strained SiGe has attracted much attention recently because of its hole mobility enhancement and compatibility with current Si technology.$^{1,2}$ In the realm of high-speed, low-power circuits, fully depleted silicon-on-insulator (FD-SOI) MOSFET is another candidate for deep submicron devices, because of the low parasitic capacitance of the source/drain junction, high carrier mobility, simple isolation and so on.$^{3,4}$ As a consequence, a FD-SOI pMOSFET combined with a strained SiGe channel can be one of the most promising p-channel device designs for improved CMOS performance.$^5$

A high-quality gate oxide is essential in FD-SOI pMOSFET devices. In conventional thermal oxidation of SiGe, the preferential oxidation of Si leads to the formation of Ge-rich layers at the oxide/substrate interface and results in serious degradation of the oxide properties.$^{6,7}$ On the other hand, aggressive MOSFET device scaling in Si has led to an interest in the deposition of high dielectric constant (high-$k$) gate materials having low leakage current and good thermal stability comparable to those of a SiO$_2$/Si interface. Replacing the thermally grown SiO$_2$ with a deposited high-$k$ dielectric also provides a viable solution in SiGe pMOSFETs because of the absence of the high-temperature SiGe oxidation process. Recently, Cho et al.,$^8$ Lee et al.,$^9$ and Mahapatra et al.$^{10}$ reported the use of high-$k$ HfO$_2$ or ZrO$_2$ layers as gate dielectrics on SiGe. However, they are vulnerable to recrystallization at high temperature during annealing, which in turn may induce higher leakage current and severe boron penetration. On the other hand, Al$_2$O$_3$ ($k=9$) films have been reported to remain amorphous even at an annealing temperature of up to 1000 °C.$^{11}$ Meanwhile, it is thermodynamically stable with Si, its band gap ($E_g=8.8$ eV) is very close to that of SiO$_2$ ($E_g=9$ eV) with adequate conduction and valence band offsets, and it is a good barrier to ionic transport.$^{12}$ These favorable properties of Al$_2$O$_3$ make it a potential high-$k$ candidate. In this article, we present the thermal annealing effects on the structure and electrical properties of the Al$_2$O$_3$ gate dielectric film grown on FD strained SiGe on insulator (SGOI) and describe the resulting interfacial reactions. The dependence of the electrical properties on the interfacial layer (IL) is also investigated by the high frequency capacitance voltage ($C$-$V$) technique. High-resolution x-ray photoelectron spectroscopy (HRXPS) results show the IL com-

---

a)Also at Department of Physics and Materials Science, City University of Hong Kong, Hong Kong, China.
b)Author to whom correspondence should be addressed; electronic mail: paul.chu@cityu.edu.hk
posed of a mixture of SiO$_x$ and GeO$_x$ at the initial growth stage. The GeO$_x$ layer is significantly reduced to Ge with increasing annealing temperature, while an interfacial silicate layer is formed after annealing.

II. EXPERIMENTAL PROCEDURES

The FD-strained SGOI substrate was fabricated by the oxidation/condensation technique. Strain relaxation is suppressed by setting the initial SiGe thickness to be less than a critical value, as proposed by Tezuka et al. In this way, the SGOI substrate with 26.7 nm thick strained SiGe channel layer, which is thin enough to operate in the FD mode, can be obtained. Afterwards, Al$_2$O$_3$ was deposited on the SiGe channel layer by conventional ultrahigh vacuum electron-beam evaporation using a high purity sintered powder target. The substrates were kept at room temperature and the main chamber was evacuated to 10$^{-6}$ – 10$^{-7}$ Pa. The growth rate was 0.3–0.5 nm/s. Postannealing was conducted under N$_2$ at 800 °C for 30 min. SGOI-metal-oxide-semiconductor (MOS) capacitors were formed by electron-beam evaporation of Al on the gate dielectric/SGOI to form the top and bottom electrodes.

III. RESULTS

Atomic force microscopy (AFM) is utilized to observe the surface morphology. The samples are scanned over an area of 5 × 5 μm$^2$, and the root-mean-square (rms) roughness and average roughness values are calculated from the images. Figures 1(a) and 1(b) display the surface morphology of the Al$_2$O$_3$ gate dielectric on SGOI before and after annealing. The rms roughness values calculated from the as-deposited and annealed samples are 1.0 and 0.92 nm, respectively. In contrast to other high-k materials with lower crystallization temperature, the annealing treatment does not lead to a rougher and coarser surface morphology from crystallization of the grains. The Al$_2$O$_3$ gate dielectric remains amorphous after high-temperature annealing, which is consistent with the following TEM results.

The thickness and structure of Al$_2$O$_3$ and the IL are first investigated using high-resolution transmission electron microscopy (HRTEM). Figure 2 shows the HRTEM micrograph of the annealed Al$_2$O$_3$ film on the FD SGOI substrate, clearly depicting the presence of amorphous Al$_2$O$_3$ with an amorphous IL. The two interfaces are observed to be atomically sharp, and the Al$_2$O$_3$ film remains amorphous after annealing (confirmed by convergent beam electron diffraction). Avoidance of recrystallization is crucial for gate dielectrics, because the grain boundaries in crystallized gate dielectrics can be the easy paths for leakage current and oxygen and dopants diffusion. The thicknesses of the Al$_2$O$_3$, IL, and SiGe layers are found to be ~9.4, ~2.3, and ~26.7 nm, respectively. The clear lattice structure without microtwins or dislocations indicates that a high-quality SGOI substrate has been fabricated using the oxidation/condensation technique. Since the IL between the Al$_2$O$_3$ and FD SGOI is an integral part of the dielectric stack, the characteristics of this layer must be investigated along with those of the Al$_2$O$_3$ film.

The microstructure of the interfacial layer is characterized using HRXPS. Figure 3 shows the Al, O, Ge, and Si concentrations (sputtering rate of ~0.25 nm/cycle) of Al$_2$O$_3$ high-k gate dielectric fabricated on a FD SGOI substrate. The Al$_{2p}$
and O$_{1\alpha}$ signals in the first 42 sputtering cycles indicate the formation of a nearly stoichiometric Al$_2$O$_3$ film. From the Al$_{2p}$, O$_{1\alpha}$, Ge$_{2p3/2}$, and Si$_{2p}$ signals, it is clear that the interfacial layer does not consist of pure SiO$_2$, but rather includes Al and Ge atoms, the signature of an Al-germano-silicate phase. It should be noted that the Si content in the interfacial region is much larger than that of Ge. The Al concentration in the interfacial region is graded from the bottom of the Al$_2$O$_3$ layer to the SiGe surface. On the contrary, the Si concentration shows an opposite trend, and the average concentrations of Al and Si in the IL are about 9%–10% and 37%–38%, respectively. That IL obtained by electron-beam evaporation has a lower Al concentration and a larger Si concentration near the SiGe surface is a big advantage for fabricating high-quality SiGe MOS transistors, and we are doing more work in this area.

In order to determine the chemical structure of the IL between the Al$_2$O$_3$ film and SiGe surface, we study the Ge$_{2p3/2}$, Si$_{2p}$, and Al$_{2p}$ signals at the interfacial region in Fig. 4. The Gaussian-Lorentzian line shapes are used to deconvolute the spectra after standard Shirley background subtraction. For comparison, the degree of freedom degree for deconvolution of the Ge$_{2p3/2}$ or Si$_{2p}$ signal in Fig. 4 is the same for the as-deposited and annealed samples. In Fig. 4(a), the high-energy part of the Ge$_{2p3/2}$ peak (i.e., at higher energies than the 1217.2 eV main peak, which is related to the Ge$^0$ state of the SiGe layer) indicates that Ge suboxides exist in the IL of the as-deposited sample. After annealing, the relative intensity of GeO$_2$ diminishes significantly. On the contrary, the relative intensity of the Si suboxides, silicate, and SiO$_2$ components of the Si$_{2p}$ spectrum greatly increases, from 43.0% before annealing to 57.5% after annealing (relative intensities are normalized against total Si intensity), as shown in Fig. 4(b). From this comparison, we can infer that the oxidation of Ge occurs readily at the growth temperature, leading to a mixture of Si and Ge oxides at the Al$_2$O$_3$/SiGe interface. After annealing, the relative intensity of GeO$_2$ diminishes significantly, whereas that of Si suboxides, silicate, or SiO$_2$ increases. In addition to the relative intensity change of the Si 2p core-level spectrum, the chemical shifts after annealing show that there are no noticeable variations with regard to Si$^{0}$, Si$^{1+}$, Si$^{2+}$, and Si$^{4+}$, which is different from the usual Si$^{3+}$ oxidized component. An additional oxidation state Si$^{4+}$ appears between Si$^{4+}$ and Si$^{3+}$ in the IL after annealing (this does not mean that we exclude the presence of the Si$^{3+}$ component in the annealed sample, but the corresponding contribution is simply overlapped by the Si$^{4+}$ one due to our limited energy resolution). It is shifted by 0.8 eV to a lower binding energy relative to Si$^{4+}$ and 3.3 eV to a higher binding energy to Si$^{3+}$. The latter value is clearly much larger than that of the as-deposited film, and even larger than the greatest value (2.65 eV) reported for Si$^{3+}$ in a conventional SiO$_2$/Si interface. It should be noted that due to the difference in the Al$_{2p}$ peak position between the as-deposited and annealed samples, a lower energy peak at 74.3 eV and a higher energy peak at 74.8 eV emerge in Fig. 4(c).

IV. DISCUSSION

By comparing the HRXPS results in Fig. 4, it can be concluded that the formation of GeO$_2$ during the initial growth stage suppresses the formation of Si suboxides, silicate, or SiO$_2$ in the IL. However, extensive SiO$_2$ and silicate formation occurs after annealing because of the reduction of GeO$_2$ to Ge. To explain the disappearance of GeO$_2$, inference may be made from the larger negative Gibbs free energy to form SiO$_2$ compared to GeO$_2$. Considering the temperature influence on the Gibbs free energy change ($\Delta G = \Delta H - \Delta TS$), the reaction GeO$_2$(cr) + Si(0) $\rightarrow$ SiO$_2$(cr) + Ge(cr) should introduce a more negative $\Delta G$ as the temperature increases. From the perspective of thermodynamics, reduction of GeO$_2$ to Ge is more spontaneous when the annealing temperature reaches 800 °C, resulting in further formation of Si suboxides, silicate, or SiO$_2$. This conclusion can also be confirmed by the relative intensity change of the Si 2p core-level spectrum in Fig. 4(b). Meanwhile, an additional oxidation state Si$^{4+}$ appears between Si$^{4+}$ and Si$^{3+}$ after annealing. As Renault et al. have indicated, this oxidation state is related to Al silicate and is assigned to Si–O–Al bonds formed from the interfacial Si$^{4+}$ oxidation state. The origin of the shift to lower binding energy, when moving from the Si$^{4+}$ to the Si$^{3+}$ oxidation state, is believed to arise from the second-nearest-neighbor change from Si to Al. The lower Pauling’s electronegativity of Al relative to Si (1.6 vs 1.9) yields enhanced charge transfer from the Al atoms to the silicate Si–O bonds, as compared to the O–Si–O situation, thereby leading to a shift of the Si$_{1s}$ core level in Si–O–Al to lower binding energy relative to SiO$_2$. Such a shift is consistent with the chemical shift of the Al$_{2p}$ core-level spectra being in opposite direction with respect to the Al–O bonds in the as-deposited sample, as indicated in Fig. 4(c). The shift of the Al$_{2p}$ peak in the annealed sample to higher binding energy because of charge transfer further proves that a silicate layer is formed after annealing at 800 °C in N$_2$ ambient. In addi-
tion to the peak shift, a reduction in Al$_{2p}$ peak is also observed in the annealed sample. It may come from the change of Al content in the IL during annealing.

The $C$-$V$ (1 MHz) characteristics of the as-deposited and postannealed Al$_2$O$_3$ film with an IL on the SGOI substrate are shown in Figs. 5(a) and 5(b), respectively. In Fig. 5(a), the hysteresis loop in the counterclockwise direction with a flatband voltage shift ($\Delta V_{FB} = 0.36$ V) indicates that a large number of interfacial trapped charges exist in the IL because of GeO$_x$ formation in the IL as shown in the Ge$_{2p3/2}$ X-ray photoelectron spectroscopy (XPS) results. On the other hand, a well-behaved $C$-$V$ curve is obtained from the annealed sample, as shown in Fig. 5(b). The trapping and detrapping electrons almost disappear, and no obvious hysteresis exists.
between the positive and negative scans indicating that little interfacial trapped charges are located in the gate dielectric or at the interface between the gate dielectric and the top SiGe of FD SGOI. We believe that this difference between the as-deposited and annealed samples mainly stems from the chemical state of the IL because of GeO\textsubscript{x} incorporation into the IL of the as-deposited film, while that of the annealed sample is largely composed of a silicate layer. According to the relationship between the density of interface states \(N_d\) and the flatband voltage shift \(\Delta V_{fb}\) in a conventional MOS capacitor, i.e., \(N_d = C_{ox} \Delta V_{fb}/q\), the reduced \(\Delta V_{fb}\) indicates that the annealing process is advantageous to the decrease in the interface state density. Another notable change between the as-deposited and annealed samples is the flatband voltage \(V_{fb}\). The reduction of GeO\textsubscript{x} to Ge during annealing results in increased Ge content near the SGOI surface, consequently modifying the band gap of SiGe leading to different values of \(V_{fb}\).

V. CONCLUSION

The interfacial characteristics and electrical properties of the Al\textsubscript{2}O\textsubscript{3} gate dielectric on FD SGOI deposited by electron-beam evaporation are investigated. An IL composed of SiO\textsubscript{x} and GeO\textsubscript{2} is observed in the as-deposited film. Interfacial silicate formation is effectively suppressed by GeO\textsubscript{2} formation at the initial growth stage. However, extensive SiO\textsubscript{x} and silicate formation occurs after annealing because of the reduction of GeO\textsubscript{2} to Ge after annealing. The formation of silicate and disappearance of GeO\textsubscript{2} lead to a decrease of the density of interfacial states and also affects the flatband voltage.

ACKNOWLEDGMENTS

This work was jointly supported by the City University of Hong Kong Strategic Research Grant (SRG) 7001820, Shanghai Rising-Star Program No. 04QMX1463, the Special Funds for Major State Basic Research Projects G2000036506, and the National Natural Science Foundation of China under Grant No. 90101012 and 60476006.