Large-size $P$-type silicon microchannel plates prepared by photoelectrochemical etching

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Abstract. The influence of backside illumination and temperature on the fabrication of large and high aspect ratio silicon microchannel plates (MCPs) by photoelectrochemical (PEC) process is described. Backside illumination is provided by three 150-W tungsten halogen lamps with a feedback loop, keeping a constant current density. The backside illumination is maintained by a circulation system. Proper backside illumination and the lower temperature can provide better integrated etching conditions compared to that without illumination and temperature control. Etching under the improved conditions results in smoother undercutting and better surface topography for large (effective diameter of about 80 mm for 4-inch silicon substrates) silicon microchannel plates. Enhancing the backside illumination within the etching temperature range ensures that the aspect ratio is more than 40, boding well for applications of silicon microchannel plates. © 2009 Society of Photo-Optical Instrumentation Engineers. (DOI: 10.1117/1.3158616)

Subject terms: silicon microchannel plates (MCPs); photoelectrochemical (PEC) etching; backside illumination; temperature.

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1 Introduction

Microchannel plates (MCPs) are two-dimensional (2-D) arrays of microscopic channel electron multipliers. Since the discovery of the peculiar optical properties of microporous Si by Canham$^{1}$ and Lehmann and Gosele$^{2}$ in 1990, the devices have been used in many low-level signal detection and imaging applications, including night vision and x-ray diagnostic systems.$^{3}$ These microchannel structures also have numerous potential applications in micro-total analysis systems, microheat exchange devices, microchemical reactors, and so on. A schematic diagram of the microchannel plates is shown in Fig. 1. Silicon microchannels usually have small size, low noise, and long stability. Because electron multiplication is realized by the avalanche effect of the secondary electrons generated from electrons impacting the wall of the channel, the ratio of the length over the width, $\alpha=L/d$ or the aspect ratio, of the channel is very important. A higher aspect ratio gives rise to higher probability of electron impact and generation of tertiary or quaternary electrons. The gain of the channel is also directly proportional to $\alpha^2$. (Ref. 4) According to Beetz et al., $\alpha$ is typically between 40 and 100. Hence, it is believed to be necessary to make the MCPs with an aspect ratio over 40. Silicon microchannel technology based on electrochemical etching originates from macroporous silicon technology and has the advantage of high aspect ratio as well as simple and low-cost equipment. Therefore, this method has also been explored widely with respect to the fabrication of silicon photonic crystals, micromachined devices, and wafer interconnection for 3-D integration.$^{2,3,9}$

However, the cost to make perfect silicon MCPs is still high even though the first report of the formation of large macropores on $p$-type silicon electrodes was published at the end of the last century.$^{10,11}$ For instance, the backside thinning process is quite costly. After etching, the upper part of the silicon wafer is turned into a microchannel structure, which is called a microchannel layer. The backside thinning process is used to remove the remaining silicon wafer on the back. However, the layer is more fragile than the silicon wafer, and the microchannel layer can be destroyed during the thinning process. For example, when a 200-$\mu m$-thick microchannel layer is etched from a 500-$\mu m$-thick silicon wafer, it is rather difficult to protect the microchannel layer from being destroyed during the removal of 300 $\mu m$ of silicon. It is even more difficult when removal approaches the microchannel layer. Furthermore, removing several hundred micrometers of materials is very time consuming. If an alternative process can form a gap between the microchannel layer and silicon substrate...
by self-undercutting during etching, it will be possible to obtain the microchannel structure directly without the need for backside thinning. The typical scanning electron microscopy (SEM) picture of the self-undercut is shown in Fig. 2. In our previous work, a microchannel layer as large as 18 mm in diameter with a high aspect ratio was produced by an undercutting process. However, it was found that such a process failed if the samples size exceeded a diameter of 25 mm. The MCP structure was often destroyed during the photoelectrochemical (PEC) etching process. Our results also indicated that the substrate temperature played an important role in the electrochemical etching procedure.

In this paper, the influence of backside illumination and temperature condition on the fabrication of high aspect ratio and large silicon microchannels is discussed. Our latest results show that etching with backside illumination can produce a microchannel layer with a high aspect ratio by undercutting if the temperature of the electrolyte is kept around a certain value.

2 Experimental Details

The MCP was produced by photoelectrochemical (PEC) etching in which light-induced electrochemical reactions were conducted on semiconductors in contact with liquids. The light-induced creation of minority carriers in semiconductors can stimulate spatially selective or material-selective etching and deposition reactions. The formation process of macroporous silicon is shown in Fig. 3. The starting substrate was 525-μm-thick single-side polished p-type Si with a resistivity of 2 to 8 Ω·cm. The surface plane was tilted 7-deg tilt to the (100) plane to meet the requirement of MCP. A silicon dioxide layer (300 nm thick) was first grown on the wafer by thermal oxidation. The oxide layer on the front side was patterned by a standard photolithographic process. Wet etching was performed in a buffered hydrofluoric acid (BHF) to open the windows [Fig. 3(b)]. Pyramidal notches serving as hole nucleation centers for anodizing were created by tetramethyl ammonium hydroxide (TMAH: 25 wt%) etching at 85 °C for a few minutes [Fig. 3(c)]. The SiO2 layer [Fig. 3(d)] was subsequently removed, and the microchannel structure was formed by electrochemical etching in hydrofluoric acid (HF) diluted with dimethylformamide (HF/DMF) [Fig. 3(e)]. The applied floating voltage was in a range of 15 to 25 V. The wafer backside was illuminated by one or three 150-W tungsten-halogen lamps and a feedback loop was employed to keep the current density constant. The temperature was kept low by a circulation system.

In the anodization process, the hole concentration plays an important role in the resulting geometrical shape. The first stage of the TMAH treatment of the concave pyramid, which determines the subsequent charge distribution around the tips, is one of the key factors to the morphology of the pore. The concentration of the electrolytes and current density in electrochemical etching are the other two key factors. In order to obtain deep channels of good quality, the electrolyte has to be within a certain range (1 to 4 mol·L⁻¹), the current density has to be at a high level (e.g., about 6 to 8 mA·cm⁻²), and last but not least, illumination is very important. It is very difficult to achieve high aspect ratio with smooth self-undercutting during etching without backside illumination.

3 Results and Discussion

In the first step, the suitable photoelectrochemical etching parameters were determined on a smaller silicon size, that is, a diameter of 18 mm. Figures 4(a) and 4(b) depict the SEM surface topography and cross section of the 18-mm-diam MCP sample, respectively. The sample was etched in a 2-mol·L⁻¹ electrolyte with a current density of 7.0 mA·cm⁻², and the backside was illuminated by one 150-W 15-V OSRAM halogen lamp. The distance between the lamp and etching cell was 14 cm. In our experiments, the lamp and etching device were attached to a certain place on the platform so that the distance and angle of illumination are constant. As shown in Fig. 4(a), the pore
diameter is 5.0 μm, and the thickness of sidewall is 1.0 μm. An aspect ratio larger than 30:1 is achieved, as shown in Fig. 4(a). In addition, the upper surface topography and sidewall of the MP sample is smooth, but the self-undercut surface (down surface) is not smooth, revealing a sawtooth structure.

The optimal experimental parameters were used to etch the 100-mm wafer. In the etching process, the etching current was controlled by altering the illumination voltage. Considering that the diameter of the sample for anodization was larger, the illumination voltage was raised to the limit. The resulting MCP sample exhibits a different color discernible by the naked eyes, as shown schematically in Fig. 5(a). The inner region (region A) with a diameter of about 20 mm shows a deep black color. The outside region (region C) shows a light black or gray color. Between (region B), the color gradually changes from deep black to gray toward the outside region. In order to explain the varying color, SEM was used to characterize the microstructures in the different regions. Figs. 5(b)–5(d) display the SEM surface topography in regions A, B, and C on the 100-mm MCP sample, respectively. Figure 5(b) shows the surface of the inside region (region A). The MCP structure is good, revealing a smooth surface on the sidewall. However, the periodic MCP structure on the surface in the outer region (region C) is completely destroyed during anodization as shown in Fig. 5(d). With regard to region B between A and C, the surface periodic MCP structure is also destroyed, but the sidewall is not destroyed, as shown in Fig. 5(c). Figures 5(e) and 5(f) depict the SEM cross-section images of regions A and C, respectively. A dense MCP array can be clearly observed in region A. On the other hand, the surface layer in region C is about 100 μm thick and the periodic MCP structure is completely destroyed. In addition, the depth of the MCP in region C is about 150 μm and not as large as that in the inner region (region A), which can reach a depth of about 200 μm. More importantly, the results clearly disclose that self-undercutting does not appear in the outer region (region C), as shown in Fig. 5(f).

The different microstructures and properties observed from regions A, B, and C are due to the different illumination intensities. As show in Fig. 6(a), a plane illumination intensity of the 150-W 15-V halogen lamp was measured by the photometer at a distance of 10 cm from the lamp. The experimental results (dots) can be fitted well by the Gauss function (solid line). The experimental results indicate that the plane illumination intensity can reach larger than 3 Klux at a distance of about 2 cm from the middle point (the maximum intensity). Then, the light intensity decreases outside this region, and the farther it is away from the middle point, the smaller is the light intensity. This is believed to be due to the inhomogeneous light intensity. The experimental results also indicate that a better MCP microstructure can be obtained with a larger illumination intensity.
To improve the illumination effect, a triple-lamp system was designed to enhance the light intensity. At the same time, an equilateral triangular structure was selected to achieve better light intensity uniformity in the triple-lamp system. The plane illumination intensity of a 150-W 15-V halogen lamp still has the Gaussian function, as shown in Fig. 6a, and the Gaussian function is used to determine the suitable distance between the lamps. As shown in Figs. 6b–6d, the larger area with uniform light intensity is obtained at a distance between lamps of about 6.5 cm. The region of uniform light intensity can be as large as a circle with a diameter of 8.0 cm, as shown in Fig. 6c. At smaller or larger distances, the results are worse. The congregated light intensity appears at a distance of 6 cm between lamps, as shown in Fig. 6b, and the dispersed light intensity appears at a distance of 7 cm between lamps, as shown in Fig. 6d. In this case, the light intensity in the triple-light illumination system can reach about 50 Klux during the etching process and it can be controlled by the lamp voltage. The real picture of the illumination system is shown in Fig. 6e.

Moreover, during etching, the current is controlled by altering the illumination voltage using software. Figure 7 shows the curve of the illumination voltage and etching current under a constant 7-V bias voltage. Table 1 shows the relationship between the illumination voltage and intensity. In the experiments, the current density is usually set to a high level of about 6 to 8 mA.cm⁻². A higher current density may help to increase the etched depth and etching rate. Hence, according to Fig. 7, it is necessary to have a lamp that can produce an intensity of more than 50 Klux in order to provide a high enough current density during etching. However, the etching rate is not believed to be linearly...
proportional to the etching current density. Simply increasing the current to extremely high levels does not necessarily produce a better microchannel structure, and the time for etching will not decrease remarkably as well. Actually, it will destroy the surface and sidewall of the MCP.

In order to fathom the influence of the illumination intensity, Fig. 8 shows the I–V curve acquired at room temperature with different illumination intensities (12.4 and 44.8 Klux at the center measured at 6.5 cm from the lamp).

Table 1 Relationship between illumination voltage and intensity.

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<thead>
<tr>
<th>Illumination voltage (V)</th>
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<tr>
<td>4</td>
<td>&lt;environment</td>
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<td>4.5</td>
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<td>5</td>
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<td>5.5</td>
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<td>6</td>
<td>12.4 K</td>
</tr>
<tr>
<td>6.5</td>
<td>17.7 K</td>
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<tr>
<td>6.75</td>
<td>20.5 K</td>
</tr>
<tr>
<td>7</td>
<td>24.5 K</td>
</tr>
<tr>
<td>7.25</td>
<td>28.4 K</td>
</tr>
<tr>
<td>7.5</td>
<td>34.2 K</td>
</tr>
<tr>
<td>7.75</td>
<td>38.2 K</td>
</tr>
<tr>
<td>8</td>
<td>44.8 K</td>
</tr>
<tr>
<td>8.5</td>
<td>59.7 K</td>
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<td>9</td>
<td>75.0 K</td>
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Note: K = 1000.

Fig. 7 Current and illumination voltage curve acquired under a constant bias voltage.

Fig. 8 I–V curves acquired under different illumination.

Fig. 9 The surface topography of the sample made by the triple-lamp system without temperature control.

Fig. 10 I–V curves obtained at different temperatures.
It can be observed that the illumination intensity indeed influences the etching current density. By using a similar method of analysis, the curve can be divided into three parts: linear region, saturated region, and avalanche region. It has been pointed out that the offset point should be selected at the saturated region, where the current is comparatively stable and injection of holes is continuous. In this case, the I–V curve is obtained with 12.4 Klux illumination intensity. The saturated region is considered from 7.1 to 16.5 V, where the etching current stops increasing and becomes steady at about 180 mA/2.3 mA/cm². For comparison, concerning the I–V curve obtained with 44.8 Klux illumination intensity, its saturated region is from 14.0 to 27.2 V, and its saturated current is about 520 mA (6.6 mA/cm²). It can be observed that the saturated region appears in the low bias voltage and current for the lower illumination intensity. If the illumination intensity is not high enough, the bias voltage has to be set at 25 V or higher to keep the higher and constant current density. In this case, the etching voltage frequently falls into the avalanche region. In the avalanche region, the kinetic energy of some carriers is high enough to break atomic bonds forming electron and hole pairs. Here, the current fluctuates randomly due to carrier scattering in the space charge region (SCR). As the pore dimension is sensitive to the etching current, this will cause lateral etching, which negatively impacts the periodic MCP structure and may even destroy it, as discussed previously.

However, our first results are not as good as we expected. The surface quality is not good enough, as shown in Fig. 9. Meanwhile, the severe chemical reaction in the electric solution at the anode side, which has not happened before, becomes noticeable. It is presumed to stem from the rise in temperature. The triple-light system gradually warms up to over 40 °C during etching. Figure 10 shows the I–V curves obtained at different temperature using the same illumination (24.5 Klux) applied to the backside. The saturated etching current appears to be more stable at the lower process temperature. Even at the avalanche region, the rising trend is not observed. This may result from a decrease in the ion mobility and that the scattering rate decreases with temperature. It has been pointed out that at near room temperature, the scattering rate is directly proportional to $T^{3/2}$ (Ref. 8), and so a lower temperature reduces the scattering rate and keeps the etching current constant. Consequently, it is easier to control the pore formation.

By lowering the temperature, the system can be improved further. Figure 11(a) shows the surface of the sample etched at 17.0 °C. The temperature is lowered by a circulation system. Obviously, the surface is better pro-

Fig. 11 Samples etched at less than 17 °C: (a) surface topography; (b) cross section.
tected compared to the previous case. Moreover, sample undercutting becomes smoother and the etched depth diminishes slightly, as shown in Fig. 11(b). These changes can probably be explained by the fact that the smaller ion mobility causes a higher rate of electropolishing, which tends to smooth out the inhomogeneities at the interfaces. 15 A higher rate of electropolishing will lead to better undercut surface, but it can also give rise to lateral etching, thereby reducing the etched depth. Fluorine ions may not reach the top of the concave pyramid for the smaller ion mobility and may reduce the etching depth as well.

4 Conclusion
Backside illumination and the temperature used in the fabrication of large and high aspect ratio silicon microchannel plates are two important factors. Together with the electrolyte concentration, current density, and etching bias, they affect the degree and quality of undercutting, surface morphology, and aspect ratio. A simple scale-up by adopting multiple light sources for a larger wafer is not ideal because changes in one factor may affect the others. Proper backside illumination and temperature yield smoother undercutting, better surface quality, and an aspect ratio of over 40.

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