Silicon-on-insulator (SOI) is rapidly becoming the substrate of choice in low-power, high-speed complementary metal oxide silicon (CMOS) technology. The traditional SOI structure consists of a silicon dioxide layer sandwiched between a top thin silicon layer in which devices are built and the silicon substrate. As device dimensions shrink, the poor heat conductance of SiO₂ imposes limitations. We have recently investigated and produced novel SOI materials using alternative dielectric materials such as aluminum nitride and diamond-like carbon that possess better heat conductance to alleviate the self-heating effect. This article reviews our recent work in this area pertaining to material fabrication and characterization. A two-dimensional numerical analysis of the self-heating effect in silicon-on-aluminum nitride is also described.

Indexing Terms: silicon-on-insulator (SOI); aluminum nitride (AlN), diamond-like carbon (DLC), self-heating effect, numerical simulation
I. Introduction

Silicon-on-insulator (SOI) technology possesses many advantages over bulk silicon technology such as the reduction of parasitic capacitance, excellent sub-threshold slope, elimination of latch up, and resistance to radiation [1]. Hence, it is preferred for high-speed, high-temperature, and low-power microelectronic devices. SOI MOS (metal oxide silicon) devices employ a buried insulating thin layer usually made of silicon dioxide to electrically isolate the devices from the bulk of the semiconductor. Due to the poor conductance of SiO₂, the buried dielectric layer also thermally isolates the MOSFETs from the bulk [2]. Consequently, the heat generated in the SOI MOSFETs causes a larger temperature rise than in bulk devices under similar conditions, and the self-heating effect that results in reduced carrier mobility and corresponding decrease in the drain current transconductance and speed becomes an inherent issue for MOSFETs built in SOI. As the device geometries diminish and transconductance as well as current density increase with MOS scaling, the self-heating effect becomes more pronounced. Possible remedies include reduction of the buried oxide thickness, quasi-SOI technology [3] and so on. Unfortunately, these solutions introduce other disadvantages [4], [5].

An alternative measure is to replace the buried silicon dioxide by another dielectric layer. The potential candidates not only must possess higher thermal conductance than SiO₂ but should also be compatible with current integrated circuit fabrication technology. In this regard, two materials are potential substitutes. Aluminum nitride (AlN), which has a thermal conductivity that is about 100 times higher than that of SiO₂ (136 W/m-K versus 1.4 W/m-K) and roughly equal to that of silicon itself (145 W/m-K), has excellent thermal stability, high electrical resistance and a coefficient of thermal expansion close to that of silicon. The second candidate is crystalline diamond with a thermal conductivity about 1,000 higher than that of SiO₂ (∼2,000 W/m-K versus 1.4 W/m-K). However, its rough surface prohibits direct bonding to silicon wafers without extensive surface polishing and treatment. We have recently fabricated a SOI structure using diamond-like carbon (DLC) as the buried layer. In this paper, our recent work on these two novel SOI structures, SOAN (silicon-on-aluminum nitride) and SOD (silicon-on-diamond like carbon) is reviewed from the material and theoretical points of view.

II. Theoretical Modeling of Self Heating Effects in Silicon-on-Aluminum Nitride (SOAN)

As a first step to evaluate the self-heating effect, theoretical modeling is very useful as the simulation protocol is transparent to semiconductor technologies while providing fast turnaround and quick design time. Our analysis is carried out using a two-dimensional device simulator called MEDICI [6–8]. The device simulator MEDICI accurately describes the behavior of the MOSFET by solving the electron and hole energy balance equations consistently with other device equations such as Poisson’s equation, the continuity equations for electrons and holes, as well as the electron and hole current density equations. It is also possible to couple the electrical and thermal characteristics in the simulator.

In our simulation, a new state variable, the lattice temperature, $T_L$, is introduced. Poisson’s equation, the current continuity equations, and the heat equation are solved in a coupled manner to obtain $T_L$. Poisson’s equation is solved for the intrinsic Fermi potential $\psi$ defined by the expression [7]:

$$-q\psi = E_c - \frac{E_g}{2} - \frac{k T_L}{2} \ln \left( \frac{N_e}{N_v} \right),$$ (1)

where $E_c$ is the conduction band energy level, $E_g$ is the bandgap energy, $N_e$ and $N_v$ are the effective conduction and valence band density of states, respectively, and $k$ is Boltzmann constant. However, when the lattice temperature is not spatially constant, $\psi$ is, in most cases, no longer a solution to Poisson’s equation. In this case, Poisson’s equation should be written as [8]:

$$\nabla \cdot \varepsilon \nabla (\psi - \theta) = -q \left( p - n + N_D^+ - N_A^- \right).$$ (2)

where $n$ and $p$ are the electron and hole densities, respectively, $N_D^+$ and $N_A^-$ are the ionized donor and acceptor impurity concentrations, respectively, and $\theta$ is the band structure parameter for the material given by

$$\theta = \chi + \frac{E_g}{2q} + \frac{k T_L}{2q} \ln \left( \frac{N_e}{N_v} \right),$$ (3)

where $\chi$ is the electron affinity of the materials. The current continuity equations are:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - U_n$$ and (4)
\[ \frac{\partial p}{\partial t} = \frac{1}{q} \nabla \cdot J_p - U_p, \]  

(5)

where \( U_n \) and \( U_p \) are the net electron and hole recombination rate, respectively and \( J_n \) and \( J_p \) are the current densities [10]:

\[ J_n = q \mu_n E_n + k \mu_n (T_L \nabla n + n \nabla T_L), \]  

(6)

\[ J_p = q \mu_p E_p + k \mu_p (T_L \nabla p + p \nabla T_L). \]  

(7)

Here, \( \mu_n \) and \( \mu_p \) are the electron and hole mobility and \( E_n \) and \( E_p \) are the electric field vectors, respectively.

In the non-isothermal case, the hot carrier effects can be omitted, and it can be assumed that the electrons and holes are in thermal equilibrium with the host lattice. Hence the electron and hole temperatures are set equal to the lattice temperature. To compute the spatially dependent lattice temperature, the heat flow equation is used:

\[ \rho c \frac{\partial T_L}{\partial t} = H + \nabla (\kappa \nabla T_L), \]  

(8)

where \( \rho \) is the mass density, \( c \) is the specific heat of the material, \( H \) is the heat generation term, and \( \kappa \) is the thermal conductivity of the materials. The heat generation in the semiconductor is modeled using:

\[ H = J_n \cdot E_n + J_p \cdot E_p + H_U, \]  

(9)

where \( H_U \) is the lattice heating due to carrier recombination/generation given by:

\[ H_U = (U_{SRH} + U_{Auger} + G^{II})E_g, \]  

(10)

where \( U_{SRH} \) and \( U_{Auger} \) are the Shockley-Read-Hole and Auger recombination rates, respectively, and \( G^{II} \) is the total generation rate due to impact ionization.

Two sets of curves are generated for the cases with and without lattice temperature effects by solving the above equations. In order to use MEDICI to solve these equations, a MOS device structure is needed. The details of the relevant geometrical and technological parameters are as follows. The device has a 10\(^{18}\) cm\(^{-3}\) p-type substrate doped and n-type source and drain doping of 10\(^{20}\) cm\(^{-3}\). The channel length is 0.3 \( \mu \)m, and the thickness of the gate oxide, top silicon and buried AlN is 5 nm, 100 nm and 300 nm, respectively. The mesh structure is shown in Figure 1. For comparison, simulation is also conducted on MOS devices fabricated in bulk Si and conventional SOI using SiO\(_2\) as the buried insulator. These devices are identical except for the buried insulator. In the bulk MOSFET simulation, the dielectric layer is simply replaced by an equal thickness of silicon.

To simulate the drain leakage, the gate bias \( V_G \) is held at 0 V and the drain bias is ramped up to 3 V. This operating state tests how well the device stays at a low drain current in spite of a large drain bias. The drain leakage current simulation results are shown in Figure 2. It is well known that the leakage current due to electron-hole pair generation in the source and drain p-n junction depletion regions is larger in a bulk device than in the SOI device because the former has much thicker depletion regions. However, as shown by our curves, the bulk leakage is lower in SOI/SOAN. This is because the top silicon layers of our chosen SOI/SOAN devices are fully depleted, which means that the

**Figure 1.** The mesh structure used in MEDICI simulation.
drain depletion region is able to punch through to affect the source-channel energy barrier. Hence the barrier to electron flow between the source and drain is much lower in the SOI/SOAN device than in the bulk device, and consequently, the leakage is higher.

To simulate the drain current in the subthreshold operating state, the drain bias is held at 0.1 V and the gate bias is ramped up from 0 V to 2 V. This operating region tests how quickly the increasing gate bias turns on the device. The simulation results based on simulated threshold voltages in the bulk, SOI and SOAN devices of 0.3251 V, 0.1786 V and 0.1976 V, respectively are depicted in Figure 3. The subthreshold slopes of these devices are 135.2 mv/dec, 99.5 mv/dec and 95.3 mv/dec, respectively. It is noted that the subthreshold characteristics of the three devices are different from each other and the subthreshold slopes of the SOI/SOAN devices are better than those of the bulk device, while SOAN is slightly better than SOI.

The results can be explained as follows. In the subthreshold region, when the drain bias is fixed, the only thing the gate bias can do is to increase the channel inversion charge. In the SOI/SOAN devices, because the top silicon film thickness is less than the maximum width of the depleted layer, the inversion charge increase is confined to the silicon layer, whereas the bulk device inversion layer extends more deeply into the substrate. It is known that the farther away the inversion charge is from the gate, the less the carrier density is in the channel region. Hence the inversion charge in the silicon film of the SOI/SOAN device that contributes to the drain current is more than the charge in the bulk device. Consequently, the subthreshold characteristic of the SOI device is better than that of a bulk device. As for the slight difference in the subthreshold characteristics between SOI and SOAN, it can be attributed to the higher dielectric constant of AlN of 9.1 compared to that of SiO₂. A reasonable explanation is that the SiO₂/AlN buried layer can be considered as a parallel plate capacitor that is proportional to the dielectric constant of the materials. Because the dielectric constant of AlN is larger than that of SiO₂, the capacitance of the AlN layer is greater than that of the SiO₂ layer. This will

![Figure 2. Simulated leakage drain currents of bulk, SOI, and SOAN devices.](image1)

![Figure 3. Simulated subthreshold characteristics of bulk, SOI, and SOAN devices.](image2)
induce larger electron charges above the AlN layer. Since the subthreshold behavior is determined by the inversion charge density in the channel of the SOI/SOAN device, the subthreshold characteristic of the SOAN device is slightly better than that of a SOI device. Based on our study, the buried AlN layer does not lead to a higher leakage current and will not degrade the subthreshold characteristics in comparison with a buried oxide layer.

In simulating the output characteristics, the gate bias is held at $10 \text{ V}$ because the self-heating effect will be more obvious when the power is high. The drain bias is ramped up from 0 to 6 V. This operating region tests the high current operation and whether the self-heating effect occurs at large gate and drain biases. The simulation results are displayed in Figure 4. The SOI device shows strong negative differential resistance (NDR) when the self-heating effect is considered, but on the other hand, both the SOAN and bulk devices display weak NDR under the same conditions. Since the mobility is sensitive to temperature and decreases as the temperature rises, the drain current also diminishes due to the degradation in the mobility and emergence of NDR. It is known that the higher the self-heating effect, the more obvious NDR is. We thus examine the self-heating effect by studying the NDR on the $I_{DS}-V_{DS}$ curves and it can be concluded that the SOI device is subject to a more substantial self-heating effect than SOAN and bulk devices under the same operating conditions. Our results are consistent with those obtained by another group using a different simulator [11].

The temperature distribution obtained under the same simulation conditions is consistent with the output characteristics. Figure 5(a) exhibits the 3-dimensional (3-D) temperature distribution of the SOI device. The x and y axes represent the horizontal and vertical dimensions of the device, respectively. The temperature in the substrate is only 300 K but because of self-heating, the channel temperature rises to 540 K. The temperature distribution patterns in the SOAN and bulk devices are displayed in Figures 5(b) and 5(c), respectively. The channel temperature in these two devices decreases significantly to about 315 K, compared to 540 K in the SOI device, and it is only slightly higher than the substrate temperature. Our results indicate that the influence of self-heating effect in SOI is much more serious than in SOAN and bulk silicon, and incidentally, the same conclusion can be drawn on the basis the aforementioned output characteristics simulation. L. J. McDaid has reported a formula pertaining to the difference between the channel and ambient temperature $\Delta T_c$ [12] 

$$\Delta T_c = \frac{P_t \cdot b_t}{K_b A}$$

where $b_t$ is the thickness of the buried layer, $K_b$ is the thermal conductivity of the buried layer, and $A$ is the area over which the power is generated (taken as the effective channel length multiplied by the device width). Because of the significantly smaller thermal conductivity of SiO$_2$ (1.40 W/m·K) compared to that of bulk silicon (145 W/m·K) and AlN (136 W/m·K) at room temperature and the same thickness of the buried insulator in SOI and SOAN device, according to above formula, $\Delta T_c$ of the SOAN device is much smaller than that of the SOI device. In other words, the majority of the heat generated during the operation of the device spreads into the silicon substrate through the buried AlN layer in the SOAN device.

### III. Fabrication and Characterization of Silicon on Aluminum Nitride Structure

Using a modified direct bonding process in conjunction with hydrogen-induced layer transfer, a silicon-on-AlN (SOAN) structure has been successfully fabricated in our laboratory [13]. To fabricate the SOAN structure, the AlN-coated acceptor wafer is bonded to a Si donor wafer that has been implanted with $6 \times 10^{16}$ cm$^{-2}$ hydrogen at 150 kV. The following measures are taken to increase the transferred area and yield of the process:

![Figure 4. Simulated output characteristics of bulk, SOI, and SOAN devices.](image-url)
A very thin (about 1 nm) Si₃N₄ film is pre-grown on the AlN-coated wafer using PECVD (plasma-enhanced chemical vapor deposition). The purpose of this layer is to change the bonding interface from AlN/Si to Si₃N₄/Si because the bonding tendency between Si₃N₄ and Si is much stronger than that between AlN and Si.

Both the acceptor and donor wafers are cleaned in the organic solvent MS2001 at 70°C for 5 mins, and then in H₂SO₄: H₂O₂ (10:1) at 120°C for 10 minutes.

Afterwards, the surfaces are activated in a 400 W oxygen plasma (oxygen pressure of 1.3 Torr) at 100°C for 1 minute.

After activation, the wafers are dipped in a modified RCA-1 solution (NH₄OH: H₂O₂: H₂O = 1: 6: 30) at 70–75°C for 60 seconds to produce a hydrophilic surface.

The two wafers are bonded using a Karl Suss SB6 VAC wafer bonder at room temperature. During bonding, a small pressure is initially applied to the center and then 1 atmospheric pressure is added onto the entire wafer for 1 min.
After bonding, the pair is heated to 120°C for 2 hours in air, and the temperature is raised to 300°C for another 10 hours to improve the bonding strength. Subsequently, the bonded wafer is furnace annealed at 450°C for 10–15 minutes under nitrogen to complete the transfer of a thin silicon layer onto the AlN-coated silicon wafer. Finally, high temperature annealing is performed in nitrogen at 1100°C for 1 hour to produce a stable SOAN structure and repair implantation defects in the top Si.

In the ion-cut process, whether or not bonding is successful is mostly determined by the low surface roughness of the AlN film. Therefore, atomic force microscopy (AFM) is performed to examine the surface topography of our AlN film, and the 5 µm × 5 µm AFM image is depicted in Figure 6. It can be observed that the surface of the AlN film is smooth and uniform with a surface roughness RMS value of 0.364 nm that is good enough for direct bonding obviating the need for complicated lapping and polishing procedures.

Figure 7 depicts a bonded wafer pair in infrared transmission showing that the entire area is bonded with the exception of a few voids. These are probably caused by residual particles trapped at the bonded interface. After splitting, a nearly entire Si thin layer is transferred onto the AlN-coated Si acceptor wafer. In order to examine the quality of the bonding interface, transmission electron microscopy (TEM) is employed. Figure 8(a) depicts the micrograph of the bonded structure giving direct evidence of the formation of the SOAN structure. The selected-area electron diffraction (SAD) patterns confirm the excellent single crystal quality of the top Si layer and amorphous structure of the buried AlN layer. The thickness of the top Si layer and buried AlN layer is about 1200 nm and 220 nm, respectively. Figure 8(b) displays the high-resolution TEM image of the interfacial region between the top Si layer and buried AlN layer. The AlN layer is homogeneous and amorphous, while the Si atoms are well aligned without showing any observable structural defects and the Si/AlN interface is as sharp as a few atomic layers. Our process is thus capable of producing nearly perfect single crystal Si on AlN. However, the Si3N4 buffer layer cannot be distinguished from this figure, which may be due to that some parts of this very thin film have been sputtered during O2 plasma activation. Besides, it is noticed that the interface between the buried AlN and Si substrate indicated in Figure 8(c) is as smooth as that between the top Si and buried AlN.

The XPS (X-ray photoelectron spectroscopy) depth profiles of Al, N, O and Si in the SOAN structure are depicted in Figure 9. The thickness of the top Si and buried AlN layers is about 1230 nm and 230 nm, respectively, which is in agreement with our TEM results. The composition with the depth of the buried layer is nearly uniform and the amount of O is observed to be below 15%, which will prohibit polycrystallization of this insulating layer during post annealing.

Spreading resistance profiling (SRP) is employed to study the electrical property of the SOAN structure and the depth profiles are illustrated in Figure 10. Three layers of the SOI structures, including the top silicon layer, buried AlN layer and Si substrate, can be readily discerned. The very steep slope from the top silicon to buried AlN at the depth of 1240 nm in the spreading resistance profile implies the sharp interface between them. The top silicon has uniform electrical properties and the buried AlN layer has an excellent insulating performance. The thickness of the top silicon and buried AlN is again in agreement with the XPS depth profile results.
IV. Fabrication and Characterization of Silicon on Diamond-Like Carbon

As aforementioned, in the ion-cut technique that involves hydrogen-induced wafer cleavage and wafer bonding, an insulator possessing higher thermal conductivity can substitute for the buried silicon dioxide. One of the interesting buried insulators is crystalline diamond with a thermal conductivity about 1000 times higher than that of SiO$_2$ (~2000 W/m·K versus 1.4 W/m·K). However, its rough surface prohibits direct bonding to silicon wafers without extensive polishing and surface treatment. In comparison, a diamond-like-carbon (DLC) thin film possesses thermal properties similar to those of crystalline diamond while retaining high electrical resistivity. Due to this unique combination of properties, a DLC buried layer can in principle outperform the buried silicon dioxide layer in SOI. We have successfully synthesized a silicon-on-DLC (SOD) structure in our laboratory using ion cutting and Si / DLC direct bonding [14].

The DLC thin films are fabricated on 100 mm $p$-type Si (100) wafers using plasma immersion ion implantation and deposition (PIII&D) [15]–[17]. During deposition, a mixture of acetylene (20 sccm) and argon (5 sccm) is bled into the chamber to a working pressure of $8 \times 10^{-4}$ Torr, and the plasma is sustained by a 500 W radio frequency (RF) source. The applied voltage, repetition rate, and pulse width are $-20$ kV, 40 Hz, and 400 $\mu$s, respectively. After deposition, some samples are furnace annealed at 500 to 1000°C in nitrogen for 1 hour whereas the other samples undergo rapid thermal annealing (RTA) at 900°C and 1000°C for 30 seconds also under nitrogen.

To fabricate the SOD structure, the DLC-coated acceptor wafer is bonded to a Si donor wafer that has been implanted with $6 \times 10^{16}$ cm$^{-2}$ hydrogen at 60 kV. Before direct bonding, both the acceptor and donor wafers are cleaned with a H$_2$SO$_4$ : H$_2$O$_2$ (10:1) solvent at 120°C for 10 minutes, followed by rinsing in de-ionized (DI) water and spin drying. The samples are then activated in oxygen plasma at 100°C for 60 seconds and dipped in a modified RCA-1 solution (NH$_4$OH:H$_2$O$_2$:H$_2$O = 1:6:30) at 70–75°C for 60 seconds, followed by DI water rinsing and spin drying again. Afterwards, the two wafers are placed with the mirror surfaces facing each other separated by three removable spacers in air at room temperature. Direct bonding occurs over the entire surface of the wafers within seconds under a small applied pressure provided by tweezers at the center after removing the spacers. After bonding, the pair is heated to 120°C for 2 hours in air, and the temperature is raised to 200°C for another 10 hours to improve the bonding strength. Subsequently, the bonded wafer is furnace annealed at 300°C for 2 hours under nitrogen and the temperature is finally raised to 450°C for 10–15 minutes to induce splitting of the thin Si layer to complete the transfer of a thin silicon layer onto the DLC-coated silicon wafer.

![Figure 8. Cross-sectional TEM images of the SOAN structure formed using direct wafer bonding and hydrogen-induced layer transfer. (a) Low magnification view of the sample. The up and bottom insets show the SAD patterns of the top Si and buried AlN, respectively. (b) HRTEM image of the interfacial region between the top Si layer and buried AlN layer indicating a defect-free and single crystal Si layer as well as an abrupt bonded interface. (c) Bottom interface between AlN layer and Si substrate that is as sharp as the upper interface shown in (b).](image-url)
Similar to our SOAN work described in the previous section, AFM is used to examine the surface topography of our as-deposited DLC film, and the $5\ \mu m \times 5\ \mu m$ AFM image is depicted in Figure 11. It can be observed that the surface of the DLC film is very smooth and uniform with a surface roughness RMS value of 0.381 nm that is good enough for direct bonding obviating the needs for complicated lapping and polishing procedures.

In addition to surface morphology, high electrical resistivity is crucial to the successful operation of devices fabricated in the SOD structure. It is common knowledge that graphitization of DLC can decrease the electrical resistivity. In order to investigate the graphitization trend in our DLC films during high temperature annealing, the breakdown electric fields of the as-deposited and annealed samples are determined. The breakdown field that reflects the insulating property of the thin film can be determined by the current-voltage ($I-V$) characteristic measured from a metal/DLC/Si MIS structure. Figure 12 shows the electrical breakdown fields of the samples as a function of annealing temperatures. The breakdown field of the as-deposited DLC film is 4.2 MV/cm which compares reasonably well with previously reported results [18]. When the samples are furnace annealed at temperatures under $900^\circ C$, the breakdown fields do not change. When the annealing temperature reaches $900^\circ C$, the breakdown field begins to decrease, but the changes are not obvious. However, when the temperature is increased to $1000^\circ C$, the breakdown field diminishes significantly. It can be inferred that graphitization of our materials does not become significant until the annealing temperature reaches $1000^\circ C$. The rapid thermal annealing (RTA) results (open circles in Figure 12) indicate that after RTA at $900^\circ C$ or $1000^\circ C$ for 20 seconds, no appreciable graphitization can be detected. Based on our results, the DLC synthesized using the special PIII&D process can withstand furnace annealing and RTA up to $900^\circ C$, making it compatible with thin film transistor (TFT) and even conventional CMOS processing.

![Figure 9. Depth profiles of Al, N, O, and Si in SOAN structure acquired by sputtering XPS.](image)

![Figure 10. Spreading resistance profile of the SOAN structure clearly showing the three-layered structure with very steep interfaces.](image)
To examine the quality of the bonding interface of the SOD structure, TEM is again employed. Figure 13(a) depicts the micrograph of the bonded structure showing direct evidence of the formation of the SOD structure. The thicknesses of top Si layer and buried DLC layer are about 550~600 nm and 100 nm, respectively. Figure 13(b) displays the high-resolution TEM image of the interfacial region between the top Si layer and buried DLC layer. The DLC layer is observed to be homogeneous and amorphous, while the Si atoms are well aligned without showing any observable structural defects. It is evident that single crystalline Si extends to the Si-DLC boundary, and the interface is as sharp as a few atomic layers. Our results clearly indicate that our process is capable of producing nearly perfect single crystal Si on DLC.

Our bonding process incorporates heating steps that give rise to chemical reactions at the interface and a higher bonding energy. A model is proposed to describe the interfacial reactions during the annealing steps in the Si-DLC bonding process. First of all, our DLC films are fabricated using a mixture of C2H2 and Ar and so the films are hydrogenated. Moreover, the H+ implanted donor silicon wafer is hydrophilic. Hence initially there exists molecular water adsorbed on the hydrophilic oxide. Water can also originate from the reaction between the two wafers

\[
\text{Si} - \text{OH} + \text{H} - \text{C} \Rightarrow \text{Si} - \text{C} + \text{H}_2\text{O}.
\]

Hence strong Si-C covalent bonds form across the interface at about $120^\circ$ C. The bonding strength of the bonded pair can be experimentally determined by measuring the crack length induced by inserting a 0.05 mm thick razor blade into the bonding interface to partially separate the pair. Our results (not shown here) indicate that the bonding strength has indeed been improved significantly after $120^\circ$ C annealing. For the sample annealed at $300^\circ$ C for 2 hrs, the bonding is sufficiently strong to withstand splitting. During these heating steps, molecular water formed from this reaction will oxidize the surrounding crystalline silicon and form molecular hydrogen via the subsequent reaction

\[
\text{Si} - 2\text{H}_2\text{O} \Rightarrow \text{SiO}_2 + 2\text{H}_2.
\]

It should be noted that the very thin SiO2 layer formed in this reaction might actually be beneficial to the electrical device properties especially if fully-depleted devices are considered. Because the thermal conductivity of DLC is several hundred times higher than that of SiO2, the very thin SiO2 will hardly affect the thermal conductivity of the total buried layer and it also serves to prevent the inter-diffusion between the top Si and buried DLC. The hydrogen gas emitted at the interface during annealing is most likely absorbed by the amorphous carbon layer [19]. However, there still exist a few interfacial bubbles in our sample in Figure 14 depicting an infrared transmission photo acquired from the $300^\circ$ C annealed pair. It is clear that with the exception of a few voids, most of the area has been bonded, and these bubbles may be due to adventitious hydrocarbons acting as nucleation sites [20].

V. Conclusion

New materials must be developed for next-generation microelectronic devices. In low-power, high-speed CMOS technology, SOI is emerging to be the substrate of choice. However, as device dimensions shrink, the self heating...
effect caused by the poor heat conductance of SiO₂ must be addressed. In this paper, our recent work on novel SOI materials made of AlN and DLC is reviewed. Our simulation reveals the advantages of using a better heat-conducting dielectric layer. Experimentally, the AlN films synthesized by our Me-PIII&D process exhibit outstanding surface topography and maintain an amorphous structure up to an annealing temperature of 1100°C. This bodes well for post annealing in CMOS processing. We have also successfully produced high-quality and heat-resistant silicon-on-DLC materials. The DLC films exhibit outstanding surface topography. The bonded interface is sharp and the top Si layer has almost perfect crystal quality. Furthermore, excellent insulating characteristics are maintained up to an annealing temperature of 900°C and this bodes well for TFT as well as CMOS processing.

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References


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