

# Electronics and Photonics Prototype Devices Based on Compound Semiconductor Nanowires/Nanobelts

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## Abstract

**We present synthesis and *in-situ* doping of several important n-type and p-type compound semiconductor 1D nanomaterials via the chemical vapor deposition method, and the nanoelectronic and nanophotonic prototype devices based on these nanomaterials. Various high performance nanoelectronic devices, including metal-insulator-semiconductor field-effect transistors (FETs), metal-semiconductor FETs, and NOT, NOR and NAND logic gates based on FETs, have been fabricated and studied. Various NW(NB)/p<sup>+</sup>-Si heterojunction electroluminescence devices have been fabricated and studied. CdS NW ring cavities were fabricated and a straight CdS NW with Fabry-Pérot cavity structure was employed to couple the light out from the ring cavity.**

## I. INTRODUCTION

Semiconductor one-dimensional (1D) nanostructures are good candidates for the building blocks of functional nanodevices such as waveguides [1-3], photoconductive optical switches [4], sensors [5], acoustic resonators [6], field effect transistors (FETs) [7,8], light-emitting diodes [9, 10], and electrically driven laser [11]. Compound semiconductor 1D nanomaterials have unique physical properties. However, unintentionally doped nanomaterials usually have high resistivities, which would limit their performance in both electronics and photonics. Therefore, finding effective ways to control doping in nanomaterials is very urgent. We have developed *in-situ* doping chemical vapor deposition (CVD) methods to synthesize high quality n-type and p-type NWs (NBs). Based on these nanomaterials, high performance metal-semiconductor field-effect-transistors (MESFETs), metal-insulator-semiconductor field-effect transistors (MISFETs), and NOT, NOR and NAND logic gates based on the FETs have been constructed. In nano photonic devices, we have fabricated and studied various NW(NB)/p<sup>+</sup>-Si heterojunction electroluminescence (EL) devices. In order to further explore the nanomaterial applications in nanophotonic systems, CdS NW ring cavities and coupled ring-Fabry-Pérot (F-P) cavity were fabricated and studied.

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## II. CURRENT RESULTS

We present that the single CdS NB MESFETs have low threshold voltage ( $\sim 1.56$  V), high transconductance ( $\sim 3.5$   $\mu$ S), low subthreshold swing ( $\sim 45$  mV/dec), and high on/off current

ratio ( $\sim 2 \times 10^8$ ). (Fig. 1) [12]. We demonstrate that the operating voltage, and the transconductance for metal-insulator-NW(NB) FETs with Si substrates as the back gate can be greatly reduced and increased, respectively, by fabricating an extra Schottky contact on the NW(NB) in the FET, and the mechanism of which is discussed [12]. Moreover, with the NW(NB) thickness reducing, the corresponding FET can even change from depletion to enhancement mode (D- and E-mode) [13]. Based on the high performance single CdS NW MESFETs, logic NOT gates (inverters) (Fig. 2(a-c)), logic NOR and NAND gates (Fig. 3(a-b)) are constructed. The inverter has a voltage gain as high as 83, which is, so far, the highest reported value for the inverters made on semiconductor NWs (NBs) [14].

Complementary metal-semiconductor (CMES) inverters are constructed with an individual n-CdS and an individual p-Zn<sub>3</sub>P<sub>2</sub> NWs on the same substrate. The NW CMES inverters have low operating voltage ( $\leq 2$  V), high voltage gain ( $\geq 7$ ), and low static power dissipation ( $\leq 0.3$  nW) [15].

High-performance D- and E-mode top-gate (T-G) MISFETs are fabricated using CdS NBs A and B with thicknesses of about 60 and 180 nm, respectively. High-k HfO<sub>2</sub> dielectric is used as the insulator layer. The threshold voltage, subthreshold swing, and on/off ratio of the CdS NB A T-G MISFET are about 0.15 V, 62 mV/dec, and  $6 \times 10^4$ , respectively. The threshold voltage, on/off ratio and peak transconductance of the CdS NB B T-G MISFET are about  $-3.4$  V,  $2 \times 10^9$ , and 11  $\mu$ S, respectively [16].

Schematic illustration for the fabrication procedure of n-ZnO NW/p<sup>+</sup>-Si heterojunctions and an FESEM image of the heterojunction are shown in Fig. 4 (a) and (b), respectively; an EL spectrum from an n-ZnO NW/p<sup>+</sup>-Si heterojunction is shown in Fig. 4(c). Sharp UV emission resulting from band-edge emission in ZnO nanowire is observed [17].

EL spectra together with the EL images from n-CdSe<sub>x</sub>S<sub>1-x</sub> NB/p<sup>+</sup>-Si heterojunctions are clearly observed. With x changing from 0–1, the EL spectrum peak changes from green to red, resulting from the band-edge emission of CdSe<sub>x</sub>S<sub>1-x</sub>.

CdS NW rings with radii from 2.1 to 5.9  $\mu$ m, and a coupled ring-F-P cavity are fabricated by a nanoprobe system installed in a scanning electron microscope. When the NW ring is excited by a focused laser, bright green light spot is observed at the output end of the straight NW, indicating that the latter had served as an effect waveguide to couple the light out from the

ring cavity (Fig. 5c). Figure 5e shows the photoluminescence (PL) spectrum collected at the output end of the straight NW with the exciting point on the NW ring, which shows that the whispering gallery modes inside the ring cavity had been modulated by the straight NW with an F-P cavity [18].

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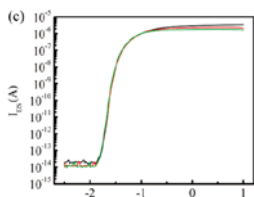


Fig. 1  $I_{DS}$ - $V_G$  curves measured at various  $V_{DS}$  (black, red, and green curves corresponding to  $V_{DS}$  of 1.0, 0.8, and 0.6 V, respectively).

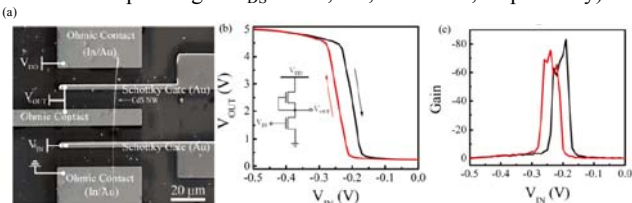


Fig. 2 (a) FESEM image of an inverter made on one single CdS NW. (b) Transfer characteristic of the inverter. Inset: the circuit diagram of the inverter. (c) The gain of the inverter vs the input voltage.

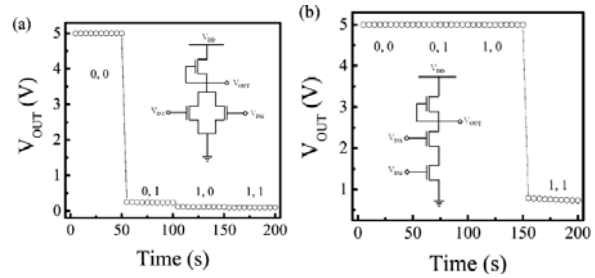


Fig. 3 (a) Output voltage of a CdS NW NOR gate for the four possible input states: (0, 0), (0, 1), (1, 0), and (1, 1). Logic input 0 is  $-0.5$  V and logic input 1 is 0 V. (b) Output voltage of a CdS NW NAND gate for the four possible input states: (0, 0), (0, 1), (1, 0), and (1, 1). Insets: the circuit diagrams of the corresponding gates.

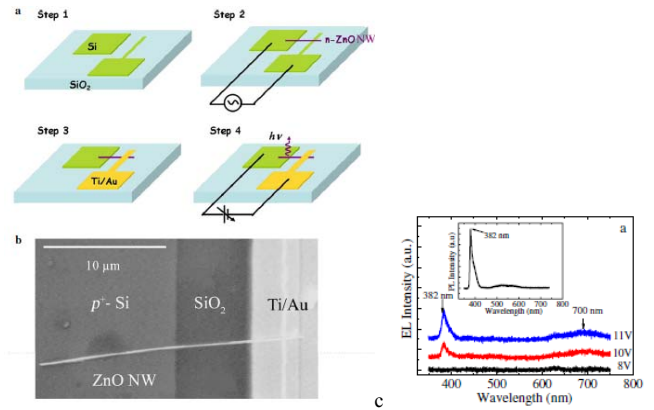


Fig. 4 (a) Schematic illustration for the fabrication procedure of n-ZnO NW/ $p^+$ -Si heterojunctions. (b) An FESEM image of an as-fabricated n-ZnO NW/ $p^+$ -Si heterojunction. (c) Room-temperature EL spectrum from an n-ZnO NW/ $p^+$ -Si heterojunction under various forward biases; the inset is PL spectrum from the NW.

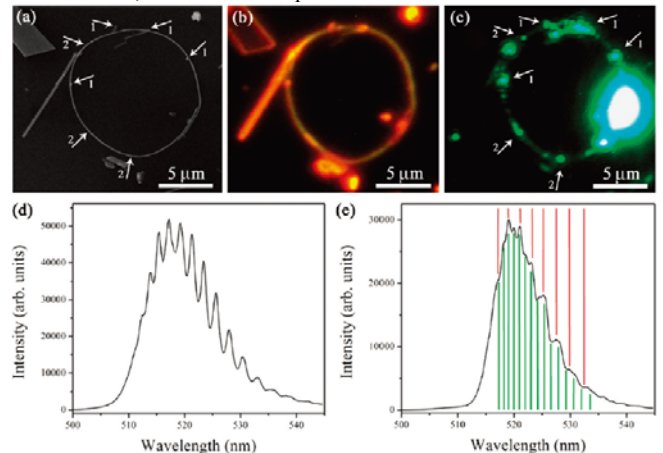


Fig. 5 (a) SEM, (b) dark field, and (c) PL image of a NW ring coupled to a straight NW. Light spots marked by arrows 1 are due to adhered particles, those marked by arrows 2 are due to defects on the NW. The corresponding positions are also marked in the SEM image in (a). (d) Spatially resolved PL spectrum of the straight NW prior to being contacted to the NW ring. (e) PL spectrum collected at the output end of the straight NW with the exciting point on the NW ring. Red and green lines mark the respective mode positions of the F-P cavity and the ring cavity.